Instruction Manual

Tektronix

TMS808
AGP4X Bus State Support

071-0560-03

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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Table of Contents

List of Figures

List of Tables

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Connect the ground lead of the probe to earth ground only.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This instruction manual contains specific information about the TMS 808 AGP4X bus support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support packages on the logic analyzer for which the TMS 808 AGP4X support was purchased, you will probably only need this instruction manual to set up and run the support package.

If you are not familiar with operating bus support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support package.

Information on basic operations of bus support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing data

Manual Conventions

This manual uses the following conventions:

- The phrase “information on basic operations” refers to the logic analyzer online help, an installation manual, or a user manual covering the basic operations of bus support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the user manual of the corresponding module. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and its associated products.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 6:00 a.m. - 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This chapter contains information on the TMS 808 AGP4X bus support and information on connecting your logic analyzer to your system under test.

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a bus in its own operating environment with little effect, if any, on the target system. Information on basic operations in your online help contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of an extender board and an interface board. The extender board includes a straddle-mount AGP4X connector that accepts the original AGP4X card. The extender board has signal conditioning circuitry on it which extracts proper digital signals from the composite wave on the transmission lines. The extender board also includes a 114-pin Mictor connector that transfers the conditioned signals to the interface board. For more detailed information on the probe adapter refer to the *Circuit description* on page 3–1.

The interface board contains digital logic which processes the AGP signals for the logic analyzer to acquire. Mictor connectors on the interface board accept P6434 probes from the logic analyzer.

The probe adapter accommodates the AGP4X bus and is powered with an external supply.

Support Package Description

The TMS 808 bus support package acquires and displays data from systems based on the Intel AGP4X bus.

To use this support efficiently, refer to information on basic operations, in your online help, and the following documents:

- *Accelerated Graphics Port Interface Specification, Intel, Version 2.0, 1998*

The AGP interface specification uses the 66 MHz PCI (*PCI Local Bus Specification*) as an operational baseline and provides four significant performance extensions or enhancements to the PCI specification which are intended to optimize the AGP for high performance 3D graphics applications. These AGP extensions are not described in, or required by, the *PCI Local Bus Specification*.

These extensions are:

- Deeply pipelined memory read and write operations, fully hiding memory access latency.
- Demultiplexing of address and data on the bus, allowing almost 100% bus efficiency.
- New AC timing in the 3.3 V electrical specification that provides for one, two, or four data transfers per 66 MHz clock cycle, allowing for real data throughput in excess of 500 MB/s.
- A new low voltage electrical specification that allows four data transfers per 66–MHz clock cycle, providing real data throughput of up to 1 GB/s.

These enhancements are realized through the use of sideband signals. The PCI specification has not been modified in any way, and the AGP interface specification has specifically avoided the use of any of the reserved fields, encodings, pins, and so on, in the PCI specification. The intent is to utilize the PCI design base while providing a range of graphics-oriented performance enhancements with varying complexity/performance tradeoffs available to the component provider.

AGP neither replaces nor diminishes the necessity of PCI in the system. This high speed port (AGP) is physically, logically, and electrically independent of the PCI bus. It is an additional connection point in the system. It is intended for the exclusive use of visual display devices; all other I/O devices will remain on the PCI bus. The add-in slot defined for AGP uses a new connector body (for electrical signaling reasons) which is not compatible with the PCI connector; PCI and AGP boards are not mechanically interchangeable.

Logic Analyzer Software Compatibility

The label on the TMS 808 support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

For use with a TLA 700 Series, the TMS 808 support requires a minimum of two 102-channel modules that are merged. Modules must be 200 MHz minimum.

Merged modules must be of the same memory depth. If not, the shallower module will determine the depth of the merged module pair. The modules must be merged before microprocessor support is loaded. The TLA 700 does not retain micro support when a merged configuration is unmerged.

Requirements and Restrictions

Review the electrical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other AGP4X support requirements and restrictions.

The AGP4X support does not have the ability to connect transferred data and the requests that generated them.

Hardware Reset. If a hardware reset occurs in your AGP4X system during an acquisition, the application may acquire an invalid sample.

System Clock Rate. The AGP4X support can acquire data from the bus operating at speeds of up to 66 MHz.

Nonintrusive Acquisition. The AGP4X microprocessor support will not intercept, modify, or present signals back to the system under test, with the exception noted under *Use of TYPEDET#*.

1.5V Operation Only. The AGP4X support can be used with only AGP4X and AGP2X 1.5 V systems. The AGP2X support will not work with 3.3 V systems. The AGP4X support will not work with 1X AGP systems. Contact Tektronix for 1X and 2X 3.3V support.

Data Transfer Rate. The AGP4X support will not work with 1X AGP systems. Contact Tektronix for 1X and 2X, 3.3V support.

Use of TYPEDET#. The TYPEDET# signal is connected to ground on the motherboard and is unconnected on the AGP4X connector. This will force the motherboard logic to use 1.5 V signaling.

AGP Modes not Verified. PIPE# mode and AGP fast writes are not tested, so Tektronix cannot guarantee functionality.

State Mode Display. The state mode waveform display must not be used to observe signals that have a repetition rate greater than the sampling frequency. For example, the AD[31:0], Strobes, SBA[7:0], and BE signals will yield incorrect values in the State mode waveform window. This is because the sampling rate is 133 MHz, where as these signals; AD[31:0], Strobes, SBA[7:0], and BE, can change at a rate of 266 MHz and may not show a steady state.

MagniVu. Timing signals displayed in groups AD[31:0] and SBA[7:0] should not be used for accurate timing measurements.

Threshold. The AGP4X support hardware uses GND-based threshold for detecting the levels, rather than using Vrefgc or Vrefcg. So a change in interface voltage levels may appear as changes in timings.

Connecting the Logic Analyzer to a System Under Test

To connect the probes to AGP4X signals in the system under test, follow these steps:

1. Power off your system under test. It is not necessary to power off the logic analyzer.

CAUTION. *Static discharge can damage the bus, the probes, and the logic analyzer module. To prevent static damage, handle these components only in a static-free environment.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the bus.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer.
3. Place the system under test on a horizontal, static-free surface.
4. Plug the probe interface board into the graphics card extender as shown in Figure 1–1 on page 1–5.
5. Secure the two boards together with the hardware provided.

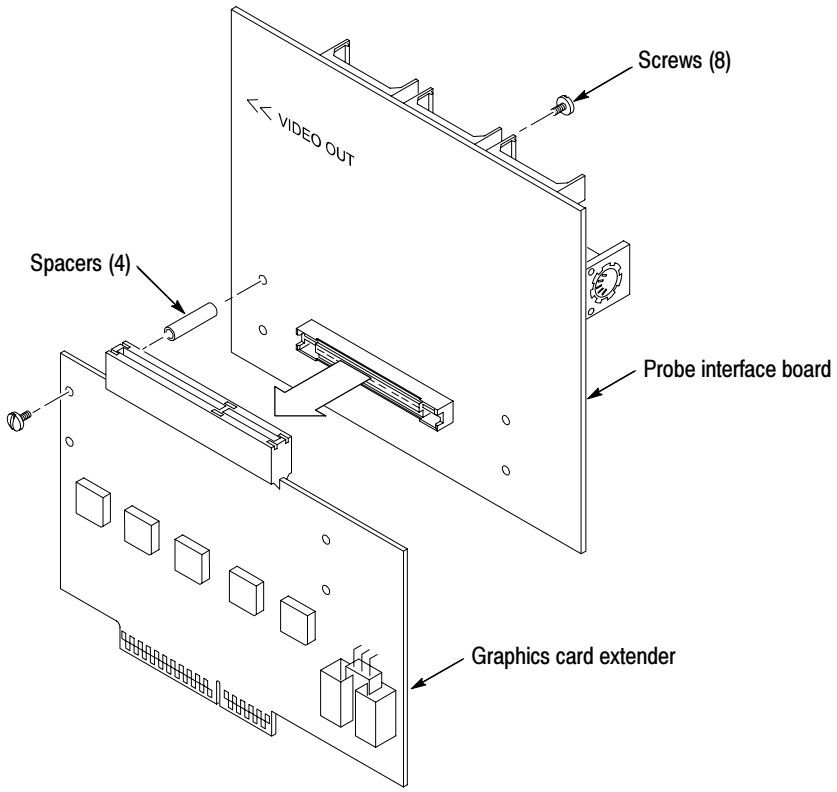


Figure 1-1: Connecting the probe adapter boards together

6. Plug the graphics card into the probe adapter. The video out silk-screen symbol on the probe interface board should point to the same side as the XGA video connector on the graphics card, as shown in Figure 1–2.

CAUTION. *To prevent damaging the graphics card, probe adapter, or system under test when power is applied, be sure to connect the AGP graphics card to the probe adapter properly .*

NOTE*. The TMS 808 product only supports 1.5V graphics cards.*

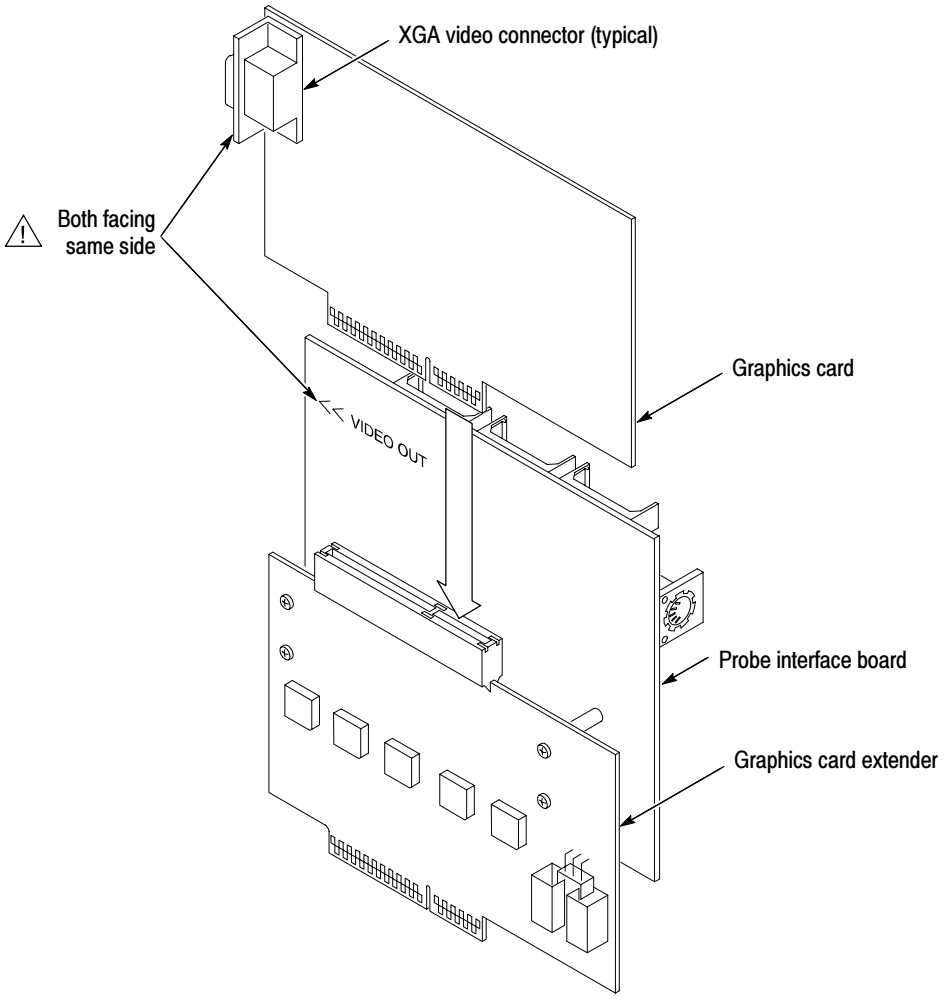


Figure 1–2: Connecting the graphics card to the probe adapter

***NOTE**. The graphics card must be plugged into the probe adapter for proper operation.*

7. Plug the probe adapter into the system under test as shown in Figure 1–3.

***CAUTION.** To prevent damaging the graphics card, probe adapter, or system under test when power is applied, be sure to connect the probe adapter to the system under test properly .*

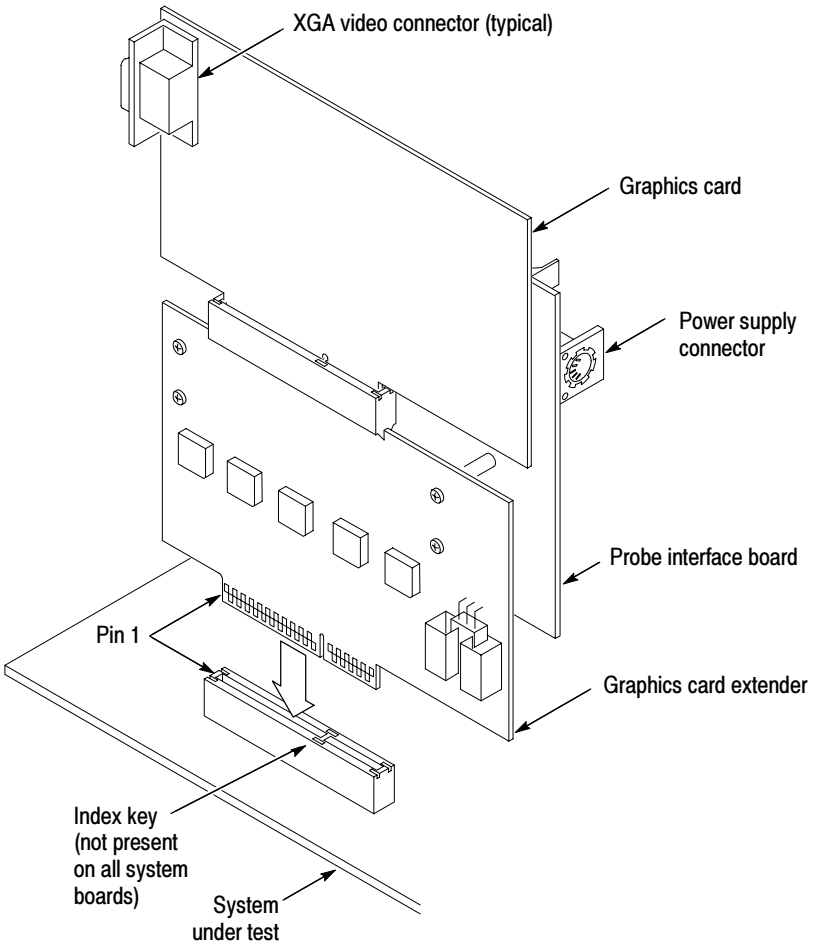


Figure 1–3: Connecting the probe adapter and graphics card to the system

8. Connect the power supply to J0290 on the probe adapter. See Figure 1–4. Plug the power supply into the appropriate AC power source.
9. Use the P6434 probes to connect to the Mictor connectors on the probe interface board. See Figure 1–4. These are connected to the signal pins as shown in Table 1–1 through Table 1–12.
10. Connect the module ends of the P6434 probes to the corresponding connectors (match label colors) on the logic analyzer. The probe module ends are keyed.
11. Apply forced air cooling across the probe adapter and AGP graphics card consistent with the recommendations of the manufacturer.

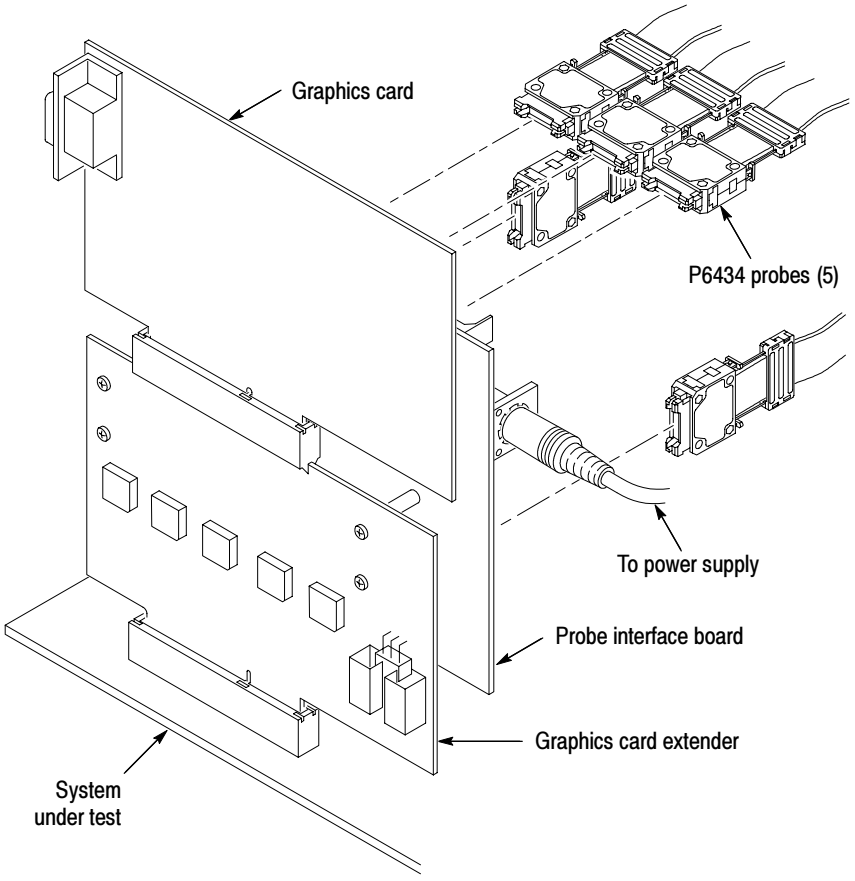


Figure 1–4: Connecting the probes to the probe adapter

12. The data transfer rate (2X or 4X) must be selected using J0590 on the probe interface board. See Figure 1–5 for jumper location and settings.

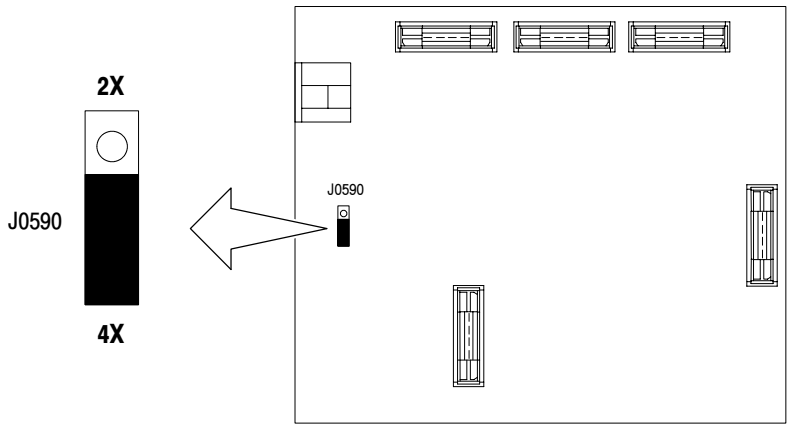


Figure 1–5: Selecting the data transfer rate

Channel Assignments

Channel assignments listed in Table 1–1 through Table 1–12 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- A pound sign (#) following a signal name indicates an active low signal.
- Channel group assignments are for all modules unless otherwise noted.
- The module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

  The TLA 704 logic analyzer has the lower-numbered slots on the top and the TLA 711 logic analyzer has the lower-numbered slots on the left.

Table 1–1 lists the probe section and channel assignments for the AD[31:0] group and the bus signal for each channel connect. By default, this channel group is displayed in hexadecimal.

Table 1–1: AD[31:0] group assignments

Bit order	Section:channel	AGP4X signal name
31	Lo_A3:7	AD31
30	Lo_A3:6	AD30
29	Lo_A3:5	AD29
28	Lo_A3:4	AD28
27	Lo_A3:3	AD27
26	Lo_A3:2	AD26
25	Lo_A3:1	AD25
24	Lo_A3:0	AD24
23	Lo_A2:7	AD23
22	Lo_A2:6	AD22
21	Lo_A2:5	AD21
20	Lo_A2:4	AD20
19	Lo_A2:3	AD19
18	Lo_A2:2	AD18
17	Lo_A2:1	AD17
16	Lo_A2:0	AD16
15	Lo_A1:7	AD15
14	Lo_A1:6	AD14
13	Lo_A1:5	AD13
12	Lo_A1:4	AD12
11	Lo_A1:3	AD11
10	Lo_A1:2	AD10
9	Lo_A1:1	AD9
8	Lo_A1:0	AD8
7	Lo_A0:7	AD7
6	Lo_A0:6	AD6
5	Lo_A0:5	AD5
4	Lo_A0:4	AD4
3	Lo_A0:3	AD3
2	Lo_A0:2	AD2
1	Lo_A0:1	AD1
0	Lo_A0:0	AD0

Table 1–2 lists the probe section and channel assignments for the AGP_Data_Hi group and the bus signal for each channel connect. By default, this channel group is displayed in hexadecimal.

Table 1–2: AGP_Data_Hi channel group assignments

Bit order	Section:channel	AGP4X signal name
31	Hi_D3:7	D_D63
30	Hi_D3:6	D_D62
29	Hi_D3:5	D_D61
28	Hi_D3:4	D_D60
27	Hi_D3:3	D_D59
26	Hi_D3:2	D_D58
25	Hi_D3:1	D_D57
24	Hi_D3:0	D_D56
23	Hi_D2:7	D_D55
22	Hi_D2:6	D_D54
21	Hi_D2:5	D_D53
20	Hi_D2:4	D_D52
19	Hi_D2:3	D_D51
18	Hi_D2:2	D_D50
17	Hi_D2:1	D_D49
16	Hi_D2:0	D_D48
15	Hi_D1:7	D_D47
14	Hi_D1:6	D_D46
13	Hi_D1:5	D_D45
12	Hi_D1:4	D_D44
11	Hi_D1:3	D_D43
10	Hi_D1:2	D_D42
9	Hi_D1:1	D_D41
8	Hi_D1:0	D_D40
7	Hi_D0:7	D_D39
6	Hi_D0:6	D_D38
5	Hi_D0:5	D_D37
4	Hi_D0:4	D_D36
3	Hi_D0:3	D_D35
2	Hi_D0:2	D_D34
1	Hi_D0:1	D_D33
0	Hi_D0:0	D_D32

Table 1–3 lists the probe section and channel assignments for the AGP_Data_Lo group and the bus signal for each channel connect. By default, this channel group is displayed in hexadecimal.

Table 1–3: AGP_Data_Lo channel group assignments

Bit order	Section:channel	AGP4X signal name
31	Lo_D3:7	D_D31
30	Lo_D3:6	D_D30
29	Lo_D3:5	D_D29
28	Lo_D3:4	D_D28
27	Lo_D3:3	D_D27
26	Lo_D3:2	D_D26
25	Lo_D3:1	D_D25
24	Lo_D3:0	D_D24
23	Lo_D2:7	D_D23
22	Lo_D2:6	D_D22
21	Lo_D2:5	D_D21
20	Lo_D2:4	D_D20
19	Lo_D2:3	D_D19
18	Lo_D2:2	D_D18
17	Lo_D2:1	D_D17
16	Lo_D2:0	D_D16
15	Lo_D1:7	D_D15
14	Lo_D1:6	D_D14
13	Lo_D1:5	D_D13
12	Lo_D1:4	D_D12
11	Lo_D1:3	D_D11
10	Lo_D1:2	D_D10
9	Lo_D1:1	D_D9
8	Lo_D1:0	D_D8
7	Lo_D0:7	D_D7
6	Lo_D0:6	D_D6
5	Lo_D0:5	D_D5
4	Lo_D0:4	D_D4
3	Lo_D0:3	D_D3
2	Lo_D0:2	D_D2
1	Lo_D0:1	D_D1
0	Lo_D0:0	D_D0

Table 1–4 lists the probe section and channel assignments for the BE_Hi group and the bus signal for each channel connect. By default, this channel group is displayed as binary.

Table 1–4: BE_Hi channel group assignments

Bit order	Section:channel	AGP4X signal name
3	Lo_C0:7	D_BE7
2	Lo_C0:6	D_BE6
1	Lo_C0:5	D_BE5
0	Lo_C0:4	D_BE4

Table 1–5 lists the probe section and channel assignments for the BE_Lo group and the bus signal for each channel connect. By default, this channel group is displayed as binary.

Table 1–5: BE_Lo channel group assignments

Bit order	Section:channel	AGP4X signal name
3	Lo_C0:3	D_BE3
2	Lo_C0:2	D_BE2
1	Lo_C0:1	D_BE1
0	Lo_C0:0	D_BE0

Table 1–6 lists the probe section and channel assignments for the Command group and the bus signal for each channel connect. The symbol table file name is AGP4X_Command. By default, this channel group is displayed as symbols.

Table 1–6: Command channel group assignments

Bit order	Section:channel	AGP4X signal name
6	Lo_C1:7	IRDY#
5	Lo_C2:3	FRAME#
4	CLK:0	PIPE#
3	Lo_C1:5	C/BE3#
2	Lo_C1:4	C/BE2#
1	Lo_C1:3	C/BE1#
0	Lo_C1:2	C/BE0#

Table 1–7 lists the probe section and channel assignments for the Status group and the bus signal for each channel connect. The symbol table file name is AGP4X_Status. By default, this channel group is displayed as symbols.

Table 1–7: Status group assignments

Bit order	Section:channel	AGP4X signal name
3	Lo_C2:1	GNT#
2	Hi_A0:2	ST2
1	Hi_A0:1	ST1
0	Hi_A0:0	ST0

Table 1–8 lists the probe section and channel assignments for the SBA[7:0] group and the bus signal for each channel connect. By default, this channel group is displayed as hexadecimal.

Table 1–8: SBA[7:0] group assignments

Bit order	Section:channel	AGP4X signal name
7	Lo_C3:7	SBA7
6	Lo_C3:6	SBA6
5	Lo_C3:5	SBA5
4	Lo_C3:4	SBA4
3	Lo_C3:3	SBA3
2	Lo_C3:2	SBA2
1	Lo_C3:1	SBA1
0	Lo_C3:0	SBA0

Table 1–9 lists the probe section and channel assignments for the SBA_Hi group and the bus signal for each channel connect. By default, this channel group is displayed as hexadecimal.

Table 1–9: SBA_Hi channel group assignments

Bit order	Section:channel	AGP4X signal name
7	Hi_A3:7	D_SBA15
6	Hi_A3:6	D_SBA14
5	Hi_A3:5	D_SBA13
4	Hi_A3:4	D_SBA12
3	Hi_A3:3	D_SBA11
2	Hi_A3:2	D_SBA10
1	Hi_A3:1	D_SBA9
0	Hi_A3:0	D_SBA8

Table 1–10 lists the probe section and channel assignments for the SBA_Lo group and the bus signal for each channel connect. By default, this channel group is displayed as hexadecimal.

Table 1–10: SBA_Lo channel group assignments

Bit order	Section:channel	AGP4X signal name
7	Hi_A2:7	D_SBA7
6	Hi_A2:6	D_SBA6
5	Hi_A2:5	D_SBA5
4	Hi_A2:4	D_SBA4
3	Hi_A2:3	D_SBA3
2	Hi_A2:2	D_SBA2
1	Hi_A2:1	D_SBA1
0	Hi_A2:0	D_SBA0

Table 1–11 lists the probe section and channel assignments of the Control group and the bus signal for each channel connect. The symbol table file name is AGP4X_Control. By default, this channel group is displayed as symbols.

Table 1–11: Control channel group assignments

Bit order	Section:channel	AGP4X signal name
13	CLK:1	RST#
12	Hi_A0:5	PME#
11	Hi_A0:3	RBF#
10	Hi_A1:3	SERR#
9	Hi_A1:7	PERR#
8	Hi_A1:6	PAR
7	Hi_A1:5	REQ#
6	Lo_C2:1	GNT#
5	CLK:0	PIPE#
4	Lo_C2:3	FRAME#
3	Lo_C1:7	IRDY#
2	Lo_C1:6	TRDY#
1	Hi_A1:4	DEVSEL#
0	Lo_C2:0	STOP#

Table 1–12 lists the probe section and channel assignments for the Misc group and the bus signal for each channel connect. By default, this channel group is displayed as hexadecimal.

Table 1–12: Misc channel group assignments

Bit order	Section:channel	AGP4X signal name
10	Lo_C2:7	AD_STB0
9	Lo_C2:6	AD_STB0#
8	Lo_C2:5	AD_STB1
7	Lo_C2:4	AD_STB1#
6	Lo_C1:1	SB_STB
5	Lo_C1:0	SB_STB#
4	Hi_A1:2	OVRCNT#
3	Hi_A0:4	WBF#
2	Hi_A0:7	INTA#
1	Hi_A0:6	INTB#
0	CLK:3	CLK

Table 1–13 lists the probe section and channel assignments for the D_AD_Strobe group and the bus signal for each channel connect. The default radix of this channel group is binary.

Table 1–13: D_AD_Strobe channel group assignments

Bit order	Section:channel	AGP4X signal name
1	Lo_C2:2	D_AD_STB[1]

[1] **The prefix D_ indicates that the signal is derived on the probe adapter.**

Table 1–14 lists the probe section and channel assignments for the D_SB_Strobe group and the bus signal for each channel connect. The default radix of this channel group is binary.

Table 1–14: D_SB_Strobe channel group assignments

Bit order	Section:channel	AGP4X signal name
1	Qual:0	D_SB_STB[1]

[1] **The prefix D_ indicates that the signal is derived on the probe adapter.**

Table 1–15 lists the probe section and channel assignments for the clock probes (not part of any group) and the AGP4X signal to which each channel connects.

Table 1–15: Clock and qualifier channel assignments

LA section and probe	AGP4X signal name
CLK:0	PIPE#
CLK:1	RST#
CLK:2	D_PCI_STATUS#
CLK:3	CLK
Lo_C2:0	STOP#
Lo_C2:1	GNT#
Lo_C2:2	D_AD_STB
Lo_C2:3	FRAME#
QUAL:0	D_SB_STB
QUAL:1	NC

Table 1–16 lists the AGP4X bus signals required by the Clocking State Machine (CSM) to properly strobe and log in the bus bus cycles into acquisition memory. Signals required for any probe adapter circuitry, if that circuitry is required for custom acquisition, must also be included.

Table 1–16: Channel groups required for clocking

TLA 700 channel	AGP4X signal name
Lo_A3:7–0 Lo_A2:7–0 Lo_A1:7–0 Lo_A0:7–0	AD[31:0] (AD[31:0] Group)
Hi_D3:7–0 Hi_D2:7–0 Hi_D1:7–0 Hi_D0:7–0	D_D[63:32] (AGP_Data_Hi Group)
Lo_D3:7–0 Lo_D2:7–0 Lo_D1:7–0 Lo_D0:7–0	D_D[31:0] (AGP_Data_Lo Group)
Lo_C0:7–4	D_BE[7–4] (BE_Hi Group)
Lo_C0:3–0	D_BE[3–0] (BE_Lo Group)
Lo_C1:7 Lo_C2:3 CLK:1 Lo_C1:5 Lo_C1:4 Lo_C1:3 Lo_C1:2	IRDY# FRAME# RST# C/BE3# C/BE2# C/BE1# C/BE0# (Command Group)
Lo_C2:1 Hi_A0:2–0	GNT# ST[2–0] (Status Group)
Hi_A3:7–0	D_SBA[15–8] (SBA_Hi Group)

Table 1-16: Channel groups required for clocking (Cont.)

TLA 700 channel	AGP4X signal name
Hi_A2:7-0	D_SBA[7-0]
	(SBA_Lo Group)
QUAL:0	D_SB_STB
Hi_A0:5	PME#
Hi_A0:3	RBF#
Hi_A1:3	SERR#
Hi_A1:7	PERR#
Hi_A1:6	PAR
Hi_A1:5	REQ#
Lo_C2:1	GNT#
CLK:1	RST#
Lo_C2:3	FRAME#
Lo_C1:7	IRDY#
Lo_C1:6	TRDY#
Hi_A1:4	DEVSEL#
Lo_C2:0	STOP#
	(Control Group)
CLK:0	PIPE#
CLK:1	RST#
CLK:2	D_PCI_STATUS#
CLK:3	CLK
	(Clock and Qualifiers)
Lo_C2:0	STOP#
Lo_C2:1	GNT#
Lo_C2:2	D_AD_STB
Lo_C2:3	FRAME#
	(Qualifiers)

Table 1–17 lists channel groups not required for clocking by the AGP4X support.

Table 1–17: Channel groups not required for clocking

TLA 700 channel	AGP4X signal name
Hi_A1:2	OVRCNT#
Hi_A0:7	INTA#
Hi_A0:6	INTB#
Hi_A0:4	WBF#
Lo_C2:7	AD_STB0
Lo_C2:6	AD_STB0#
Lo_C2:5	AD_STB1
Lo_C2:4	AD_STB1#
Lo_C1:1	SB_STB
Lo_C1:0	SB_STB#
Lo_C3:7-0	SBA[7-0]

Acquisition Setup. The AGP4X support will affect the logic analyzer setup menus and submenus by modifying existing fields and adding micro-specific fields.

The AGP4X support will add the selections AGP4X and AGP2X to the Load Support Package dialog box, located under the File pulldown menu. Once the AGP4X support has been loaded, the Custom clocking mode selection in the module Setup menu is also enabled.

Table 1–18 lists the signals that are available on test pads on the probe adapter, but not connected to the Mictor connectors.

Table 1–18: Signals on the probe adapter that are not acquired

AGP4X pin number	AGP4X signal name
B4	USB+
A4	USB-
A66	Vrefgc
B66	Vrefcg
A34	Vddq1.5
A28	Vcc3.3
B24	3.3Vaux
B2	5.0V
A1	12.0V

Channel Charts

Tables 1–19 through 1–26 identify the signal names assigned to the acquisition channel numbers on the logic analyzer.

Table 1–19: Clock channels

TLA clock channel	CLK or Qual	Active CLK edge	AGP4X signal name
CLK:3	CLK	Both	CLK
CLK:2	QUAL		D_PCI_STATUS#
CLK:1	QUAL		RST#
CLK:0	QUAL		PIPE#

Table 1–20: Qual channels

TLA Qual channel	AGP4X signal name
QUAL:1	NC
QUAL:0	D_SB_STB

Table 1-21: 32 Channel Address_Lo section on the lower module

TLA acquisition channel	Login group	AGP4X signal name
Lo_A3:7	LOGA7	AD31
Lo_A3:6	LOGA7	AD30
Lo_A3:5	LOGA7	AD29
Lo_A3:4	LOGA7	AD28
Lo_A3:3	LOGA6	AD27
Lo_A3:2	LOGA6	AD26
Lo_A3:1	LOGA6	AD25
Lo_A3:0	LOGA6	AD24
Lo_A2:7	LOGA5	AD23
Lo_A2:6	LOGA5	AD22
Lo_A2:5	LOGA5	AD21
Lo_A2:4	LOGA5	AD20
Lo_A2:3	LOGA4	AD19
Lo_A2:2	LOGA4	AD18
Lo_A2:1	LOGA4	AD17
Lo_A2:0	LOGA4	AD16
Lo_A1:7	LOGA3	AD15
Lo_A1:6	LOGA3	AD14
Lo_A1:5	LOGA3	AD13
Lo_A1:4	LOGA3	AD12
Lo_A1:3	LOGA2	AD11
Lo_A1:2	LOGA2	AD10
Lo_A1:1	LOGA2	AD9
Lo_A1:0	LOGA2	AD8
Lo_A0:7	LOGA1	AD7
Lo_A0:6	LOGA1	AD6
Lo_A0:5	LOGA1	AD5
Lo_A0:4	LOGA1	AD4
Lo_A0:3	LOGA0	AD3
Lo_A0:2	LOGA0	AD2
Lo_A0:1	LOGA0	AD1
Lo_A0:0	LOGA0	AD0

Table 1-22: 32 Channel Address_Hi Section on the lower module

TLA acquisition channel	Login group	AGP4X signal name
Hi_A3:7	LOGA7	D_SBA15
Hi_A3:6	LOGA7	D_SBA14
Hi_A3:5	LOGA7	D_SBA13
Hi_A3:4	LOGA7	D_SBA12
Hi_A3:3	LOGA6	D_SBA11
Hi_A3:2	LOGA6	D_SBA10
Hi_A3:1	LOGA6	D_SBA9
Hi_A3:0	LOGA6	D_SBA8
Hi_A2:7	LOGA5	D_SBA7
Hi_A2:6	LOGA5	D_SBA6
Hi_A2:5	LOGA5	D_SBA5
Hi_A2:4	LOGA5	D_SBA4
Hi_A2:3	LOGA4	D_SBA3
Hi_A2:2	LOGA4	D_SBA2
Hi_A2:1	LOGA4	D_SBA1
Hi_A2:0	LOGA4	D_SBA0
Hi_A1:7	LOGA3	PERR#
Hi_A1:6	LOGA3	PAR
Hi_A1:5	LOGA3	REQ#
Hi_A1:4	LOGA3	DEVSEL#
Hi_A1:3	LOGA2	SERR#
Hi_A1:2	LOGA2	OVRCNT#
Hi_A1:1	LOGA2	NC
Hi_A1:0	LOGA2	NC
Hi_A0:7	LOGA1	INTA#
Hi_A0:6	LOGA1	INTB#
Hi_A0:5	LOGA1	PME#
Hi_A0:4	LOGA1	WBF#
Hi_A0:3	LOGA0	RBF#
Hi_A0:2	LOGA0	ST2
Hi_A0:1	LOGA0	ST1
Hi_A0:0	LOGA0	ST0

Table 1-23: 32 Channel Data_Hi section on the higher module

TLA acquisition channel	Login group	AGP4X signal name
Hi_D3:7	LOGD7	D_D63
Hi_D3:6	LOGD7	D_D62
Hi_D3:5	LOGD7	D_D61
Hi_D3:4	LOGD7	D_D60
Hi_D3:3	LOGD6	D_D59
Hi_D3:2	LOGD6	D_D58
Hi_D3:1	LOGD6	D_D57
Hi_D3:0	LOGD6	D_D56
Hi_D2:7	LOGD5	D_D55
Hi_D2:6	LOGD5	D_D54
Hi_D2:5	LOGD5	D_D53
Hi_D2:4	LOGD5	D_D52
Hi_D2:3	LOGD4	D_D51
Hi_D2:2	LOGD4	D_D50
Hi_D2:1	LOGD4	D_D49
Hi_D2:0	LOGD4	D_D48
Hi_D1:7	LOGD3	D_D47
Hi_D1:6	LOGD3	D_D46
Hi_D1:5	LOGD3	D_D45
Hi_D1:4	LOGD3	D_D44
Hi_D1:3	LOGD2	D_D43
Hi_D1:2	LOGD2	D_D42
Hi_D1:1	LOGD2	D_D41
Hi_D1:0	LOGD2	D_D40
Hi_D0:7	LOGD1	D_D39
Hi_D0:6	LOGD1	D_D38
Hi_D0:5	LOGD1	D_D37
Hi_D0:4	LOGD1	D_D36
Hi_D0:3	LOGD0	D_D35
Hi_D0:2	LOGD0	D_D34
Hi_D0:1	LOGD0	D_D33
Hi_D0:0	LOGD0	D_D32

Table 1-24: 32 Channel Data_Lo section on the lower module

TLA acquisition channel	Login group	AGP4X signal name
Lo_D3:7	LOGD7	D_D31
Lo_D3:6	LOGD7	D_D30
Lo_D3:5	LOGD7	D_D29
Lo_D3:4	LOGD7	D_D28
Lo_D3:3	LOGD6	D_D27
Lo_D3:2	LOGD6	D_D26
Lo_D3:1	LOGD6	D_D25
Lo_D3:0	LOGD6	D_D24
Lo_D2:7	LOGD5	D_D23
Lo_D2:6	LOGD5	D_D22
Lo_D2:5	LOGD5	D_D21
Lo_D2:4	LOGD5	D_D20
Lo_D2:3	LOGD4	D_D19
Lo_D2:2	LOGD4	D_D18
Lo_D2:1	LOGD4	D_D17
Lo_D2:0	LOGD4	D_D16
Lo_D1:7	LOGD3	D_D15
Lo_D1:6	LOGD3	D_D14
Lo_D1:5	LOGD3	D_D13
Lo_D1:4	LOGD3	D_D12
Lo_D1:3	LOGD2	D_D11
Lo_D1:2	LOGD2	D_D10
Lo_D1:1	LOGD2	D_D9
Lo_D1:0	LOGD2	D_D8
Lo_D0:7	LOGD1	D_D7
Lo_D0:6	LOGD1	D_D6
Lo_D0:5	LOGD1	D_D5
Lo_D0:4	LOGD1	D_D4
Lo_D0:3	LOGD0	D_D3
Lo_D0:2	LOGD0	D_D2
Lo_D0:1	LOGD0	D_D1
Lo_D0:0	LOGD0	D_D0

Table 1-25: 32 Channel Control section (sorted by channel number) on the lower module

TLA acquisition channel	Login group	AGP4X signal name
Lo_C3:7	LOGC7	SBA7
Lo_C3:6	LOGC6	SBA6
Lo_C3:5	LOGC5	SBA5
Lo_C3:4	LOGC4	SBA4
Lo_C3:3	LOGC7	SBA3
Lo_C3:2	LOGC6	SBA2
Lo_C3:1	LOGC5	SBA1
Lo_C3:0	LOGC4	SBA0
Lo_C2:7	LOGC7	AD_STB0
Lo_C2:6	LOGC6	AD_STB0#
Lo_C2:5	LOGC5	AD_STB1
Lo_C2:4	LOGC4	AD_STB1#
Lo_C2:3%*	LOGC7	FRAME#
Lo_C2:2%*	LOGC6	D_AD_STB
Lo_C2:1%*	LOGC5	GNT#
Lo_C2:0%*	LOGC4	STOP#
Lo_C1:7	LOGC3	IRDY#
Lo_C1:6	LOGC2	TRDY#
Lo_C1:5	LOGC1	C/BE3#
Lo_C1:4	LOGC0	C/BE2#
Lo_C1:3	LOGC3	C/BE1#
Lo_C1:2	LOGC2	C/BE0#
Lo_C1:1	LOGC1	SB_STB
Lo_C1:0	LOGC0	SB_STB#
Lo_C0:7	LOGC3	D_BE7
Lo_C0:6	LOGC2	D_BE6
Lo_C0:5	LOGC1	D_BE5
Lo_C0:4	LOGC0	D_BE4
Lo_C0:3	LOGC3	D_BE3
Lo_C0:2	LOGC2	D_BE2
Lo_C0:1	LOGC1	D_BE1
Lo_C0:0	LOGC0	D_BE0

* **Indicates the channel is a qualifier**

Table 1-26: 32 Channel Control Section (sorted by login group) on the lower module

TLA acquisition channel	Login group	AGP4X signal name
Lo_C3:7	LOGC7	SBA7
Lo_C3:3	LOGC7	SBA3
Lo_C2:7	LOGC7	AD_STB0
Lo_C2:3*	LOGC7	FRAME#
Lo_C3:6	LOGC6	SBA6
Lo_C3:2	LOGC6	SBA2
Lo_C2:6	LOGC6	AD_STB0#
Lo_C2:2*	LOGC6	D_AD_STB
Lo_C3:5	LOGC5	SBA5
Lo_C3:1	LOGC5	SBA1
Lo_C2:5	LOGC5	AD_STB1
Lo_C2:1*	LOGC5	GNT#
Lo_C3:4	LOGC4	SBA4
Lo_C3:0	LOGC4	SBA0
Lo_C2:4	LOGC4	AD_STB1#
Lo_C2:0*	LOGC4	STOP#
Lo_C1:7	LOGC3	IRDY#
Lo_C1:3	LOGC3	C/BE1#
Lo_C0:7	LOGC3	D_BE7
Lo_C0:3	LOGC3	D_BE3
Lo_C1:6	LOGC2	TRDY#
Lo_C1:2	LOGC2	C/BE0#
Lo_C0:6	LOGC2	D_BE6
Lo_C0:2	LOGC2	D_BE2
Lo_C1:5	LOGC1	C/BE3#
Lo_C1:1	LOGC1	SB_STB
Lo_C0:5	LOGC1	D_BE5
Lo_C0:1	LOGC1	D_BE1
Lo_C1:4	LOGC0	C/BE2#
Lo_C1:0	LOGC0	SB_STB#
Lo_C0:4	LOGC0	D_BE4
Lo_C0:0	LOGC0	D_BE0

*** Indicates the channel is a qualifier**

Standard Accessories

The TMS 808 Support is shipped with the following standard accessories:

- TMS 808 Support SW Disk
- TMS 808 Support Instruction Manual
- TLA 700 Series Micro Installation Sheet

Options

The following options are available when ordering the TMS 808 Support:

- Option 11–Add Probe Adapter
- Option 21–Add P6434 Mass-Termination Probes (5)
- Option A1 Power Cord
- Option A2 Power Cord
- Option A3 Power Cord
- Option A5 Power Cord
- Option A99 Delete Power Cord

Troubleshooting Guide

This Troubleshooting Guide is provided to ensure that the probe adapter is functioning correctly. It is recommended that you read the following bullets.

CAUTION. *Ensure that the probe adapter is properly plugged in the correct orientation. Please note that it is possible to insert the probe adapter in a universal socket in an incorrect orientation, which may damage the probe adapter and the system under test (see Figure 1–2 on page 1–6). The label 'video out' on the probe adapter indicates the direction in which a normal display adapter would have its video out connector.*

- Make sure that power is reaching the probe adapter. To verify this, look at the green LED near the heat sink on the extender board of the probe adapter. It will be on; if it is not, it may indicate that the power adapter is not properly plugged in or powered on. If the LED is still not on, the probe adapter may have a problem that needs servicing.

- Make sure that all the Mictor connectors are plugged in correctly. The activity window (select the Show Activity button on the Setup panel) may be used to verify this. Run a test program on the system under test and verify that the signals are showing activity (toggling) as expected.
- The Show Activity window can also be used to detect which mode of AGP the system is running. When a program that uses AGP transfers is being run on the system under test, the following can be observed:
  - AD_STB0 (C2:7) toggles in the case of any AGP activity
  - SB_STB (C1:1) toggles if the system uses side band for address queuing
  - The complementary strobes AD_STB0# (C2:6) and SB_STB# (C1:0) toggle when the transfer rate is 4X (but not in 2X).
- Please note when using an AGP 2X system that you must change the jumper (J0590) on the adapter board (see Figure 1–5 on page 1–9 for J0590 location) and load the separate support package named AGP 2X. Also, the TMS 808 supports only 1.5V signaling.
- While triggering on data being transferred by AGP protocol, avoid triggering on AD bus signals. Since AD bus signals change faster than the custom sampling rate, there are chances of false triggering. Instead use AGP_Data_Hi or AGP_Data_Lo groups. Normally, the first and third data in a cycle appear on the Data_hi group.
- Signals that change state faster than the custom sampling rate when observed in the state waveform window, may appear as incorrect representations. These include the AD bus, SBA bus and the strobes.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. The information covers the following topics:

- Symbol table files
- Clocking options

The information in this section is specific to the operations and functions of the TMS 808 AGP4X support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassemble data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the AGP4X support are AD[31:0], AGP_Data_Hi, AGP_Data_Lo, BE_Hi, BE_Lo, Command, Status, SBA_Hi, SBA_Lo, Control, Misc, D_AD_Strobe and D_SB_Strobe. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–10.

Symbols

The TMS 808 support supplies four symbol table files. Each file replaces specific channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file AGP4X_Command, the Command channel group symbol table.

Table 2–1: Command group symbol table definitions

Symbol	Command group value		Meaning
	IRDY# FRAME# PIPE#	C/BE3# C/BE2# C/BE1# C/BE0#	
-	X 1 1	X X X X	Not an AGP or PCI command
Bus_Fault	X 0 0	X X X X	Bus Fault

Table 2-1: Command group symbol table definitions (cont.)

Symbol	Command group value IRDY# FRAME# PIPE#	 C/BE3# C/BE2# C/BE1# C/BE0#	Meaning
AGP_Rd_LP	X 1 0	0 0 0 0	AGP Low Priority Read
AGP_Rd_HP	X 1 0	0 0 0 1	AGP High Priority Read
AGP_Wr_LP	X 1 0	0 1 0 0	AGP Low Priority Write
AGP_Wr_HP	X 1 0	0 1 0 1	AGP High Priority Write
AGP_Lg_Rd_LP	X 1 0	1 0 0 0	AGP Low Priority Long Read
AGP_Lg_Rd_HP	X 1 0	1 0 0 1	AGP High Priority Long Read
AGP_Flush	X 1 0	1 0 1 0	AGP Flush command
AGP_Fence	X 1 0	1 1 0 0	AGP Fence command
AGP_Ext_Addr	X 1 0	1 1 0 1	AGP Extended Address command
AGP_Lg_Rd	X 1 0	1 0 0 X	AGP Long Read
AGP_Rd	X 1 0	0 0 0 X	AGP Read
AGP_Wr	X 1 0	0 1 0 X	AGP Write
AGP_Cmd	X 1 0	X X X X	Any AGP command
PCI_Int_Ack	1 0 1	0 0 0 0	PCI Interrupt Acknowledge
PCI_Special	1 0 1	0 0 0 1	PCI Special command
PCI_I/O_Rd	1 0 1	0 0 1 0	PCI Input/Output Read
PCI_I/O_Wr	1 0 1	0 0 1 1	PCI Input/Output Write
PCI_Mem_Rd	1 0 1	0 1 1 0	PCI Memory Read
PCI_Mem_Wr	1 0 1	0 1 1 1	PCI Memory Write
PCI_Config_Rd	1 0 1	1 0 1 0	PCI Configuration Read
PCI_Config_Wr	1 0 1	1 0 1 1	PCI Configuration Write
PCI_Mem_Rd_Mul	1 0 1	1 1 0 0	PCI Memory Read Multiple
PCI_Ext_Addr	1 0 1	1 1 0 1	PCI Extended Address
PCI_Mem_Rd_Line	1 0 1	1 1 1 0	PCI Memory Read Line
PCI_Mem_Rd_Inv	1 0 1	1 1 1 1	PCI Memory Write and Invalidate

Table 2-1: Command group symbol table definitions (cont.)

Symbol	Command group value IRDY# FRAME# PIPE# C/BE3# C/BE2# C/BE1# C/BE0#	Meaning
PCI_I/O_R/W	1 0 1 0 0 1 X	PCI Input/Output Read/Write
PCI_Mem_R/W	1 0 1 0 1 1 X	PCI Memory Read/Write
PCI_Config_R/W	1 0 1 1 0 1 X	PCI Configuration Read/Write
PCI_Cmd	1 0 1 X X X X	Any PCI command
~	0 0 1 X X X X	PCI data (not the last data)

Table 2-2 shows the name, bit pattern, and meaning for the symbols in the file AGP4X_Status, the Status channel group symbol table.

Table 2-2: Status group symbol table definitions

Symbol	Status group value GNT# ST2 ST1 ST0	Meaning
-	1 X X X	Grant not asserted
Grant	0 1 1 1	Transaction Request
Rd_LP	0 0 0 0	Low Priority Read
Rd_HP	0 0 0 1	High Priority Read
Wr_LP	0 0 1 0	Low Priority Write
Wr_HP	0 0 1 1	High Priority Write
Rd	0 0 0 X	Any Read
Wr	0 0 1 X	Any Write
Rd/Wr	0 0 X X	Any Read or Write
LP	0 0 X 0	Any Low Priority
HP	0 0 X 1	Any High Priority

Table 2–3 shows the name, bit pattern, and meaning for the symbols in the file AGP4X_Control, the Control channel group symbol table.

Table 2–3: Control group symbol table definitions

Symbol	Control group value RST# RBF# REQ# IRDY# PME# SERR# GNT# TRDY# PERR# PIPE# DEVSEL# PAR FRAME# STOP#	Meaning
Reset	0 X X X X X X X X X X X X	Reset
Sys_Err	1 X X 0 X X X X X X X X X	System Error
Par_Err	1 X X X 0 X X X X X X X X	Parity Error
AGP_Addr	1 X X X X X X 0 1 1 1 1 X	AGP Address
PCI_Addr	1 X X X X X X 1 0 1 1 1 X	PCI Address
PCI_Data	1 X X X X X X 1 X 0 0 0 1	PCI Data
PCI_Abort	1 X X X X X X 1 X 0 X 1 0	PCI Target Abort
PCI_Discon	1 X X X X X X 1 X 0 X 0 0	PCI Target Disconnect
IRDY_TRDY	1 X X X X X X X X 0 0 X X	IRDY/TRDY asserted
IRDY	1 X X X X X X X X 0 X X X	IRDY asserted
TRDY	1 X X X X X X X X X 0 X X	TRDY asserted
Rd_Buf_Fl	1 X 0 X X X X X X X X X X	Read Buffer Full
Grant	1 X X X X X X 0 X X X X X	Grant asserted
Request	1 X X X X X 0 X X X X X X	Request asserted
Stop	1 X X X X X X X X X X X 0	Stop asserted
Dev_Sel	1 X X X X X X X X X X 0 X	Device Select asserted
Pwr_Mgmt_En	1 0 X X X X X X X X X X X	Power Management Enable
Pipe	1 X X X X X X 0 1 X X X X	PIPE asserted
Frame	1 X X X X X X 1 0 X X X X	Frame asserted
-	1 1 1 1 1 X 1 1 1 1 1 1 1 1	Bus inactive

Table 2–4 shows the name, bit pattern, and meaning for the symbols in the file AGP4X_SBA_Cmd, the SBA_Hi Command channel group symbol table.

Table 2–4: SBA_Hi Command group symbol table definitions

Symbol	SBA_Hi Command group value D_SBA15 D_SBA14 D_SBA13 D_SBA12 D_SBA11 D_SBA10 D_SBA9 D_SBA8	Meaning
SYNC	1 1 1 1 1 1 1 0	Synchronization cycle
NOP	1 1 1 1 1 1 1 1	NOP
Type_4	1 1 1 0 X X X X	Extended address
Type_3	1 1 0 0 X X X X	Upper address
Invalid	1 1 0 1 X X X X	Invalid
Rd_LP	1 0 0 0 0 0 0 X	Read, low priority
Rd_HP	1 0 0 0 0 1 0 X	Read, high priority
Reserved	1 0 0 0 1 0 0 X	Reserved command
Reserved	1 0 0 0 1 1 0 X	Reserved command
Wr_LP	1 0 0 1 0 0 0 X	Write, low priority
Wr_HP	1 0 0 1 0 1 0 X	Write, high priority
Reserved	1 0 0 1 1 0 0 X	Reserved command
Reserved	1 0 0 1 1 1 0 X	Reserved command
L_Rd_LP	1 0 1 0 0 0 0 X	Long read, low priority
L_Rd_HP	1 0 1 0 0 1 0 X	Long read, high priority
Flush	1 0 1 0 1 0 0 X	Flush command
Reserved	1 0 1 0 1 1 0 X	Reserved command
Fence	1 0 1 1 0 0 0 X	Fence command
DAC	1 0 1 1 0 1 0 X	Dual address cycle
Reserved	1 0 1 1 1 0 0 X	Reserved command
Reserved	1 0 1 1 1 1 0 X	Reserved command
Invalid	1 0 X X X X 1 X	Invalid
Type_1	0 X X X X X X X	Lower address
Reserved	1 1 1 1 0 X X X	Reserved command

How Data is Acquired

This part of the chapter explains how the module acquires AGP4X signals using the TMS 808 software and probe adapter. This part also provides additional information on bus signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections, if any.

Custom Clocking

A special clocking program is loaded to the module every time you load the AGP4X or AGP2X support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the AGP4X bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

Although all cycle types are acquired, there are too many to illustrate in this manual. Refer to the *AGP4X Interface Specifications* for descriptions of the other cycle types.

Clocking Options

There are two field settings in the clocking options for the AGP4X and AGP2X: Address Enqueuing and Acquisition Edge. The first field is called Address Enqueuing, and its selections are as follows:

- On AD Bus Only
- On SBA Bus Only Default

The selection On AD Bus Only is used to indicate the enqueuing of the addresses using the PIPE# signal. The addresses are now available on the AD[31..0] bus in this mode. The On AD Bus Only is used whenever the AGP master (AGP4X connector) uses the AD bus in a multiplexed manner for transferring and data information.

The selection On SBA Bus Only is used to indicate the enqueuing of the addresses using the Side Band strobe signals. The addresses are now available on the SBA[7..0] bus in this mode. The On SBA Bus Only selection is used whenever the AGP master (AGP4X connector) has implemented side band signals and uses them to enqueue requests. The On SBA Bus Only selection is potentially the higher performance method; therefore, its defined as the default.

The second field is called Acquisition Edge, and its selections are as follows:

- Active Cycles Only Default
- Rising Only
- Falling Only

- Rising & Falling

The selection Active Cycles Only clocks in only those cycles which have valid data on the AD[31..0], SBA[7..0], C/BE[3-0]#, and the ST[2..0] buses. The Active Cycles Only selection is used to acquire data. In this mode the AGP4X support will correctly identify valid cycles and display them. Active Cycles Only is defined as the default.

The selection Rising Only CLK Edge clocks in all the channels on the rising edge of the AGP CLK signal. The Rising Only selection will not acquire AGP cycles correctly, but can acquire PCI type cycles, even if qualifying signals are not present.

The following selections Falling Only and Rising & Falling are used only if data capture at the particular edge of AGP clock is important, even if the qualifying signals are not present.

The selection Falling Only CLK Edge clocks in all the channels on the falling edge of the AGP CLK signal.

The selection Rising & Falling CLK Edge clocks in all the channels on both the rising and falling edges of the AGP CLK signal.

Setup/Hold Adjustment Procedure

The purpose of this Setup/Hold adjustment procedure is to determine if the Setup/Hold values need to be adjusted to remove timing violations, so that the state data will be accurately displayed on the logic analyzer. The minimum Setup/Hold requirement for logic analyzer using merged modules is 2.5 ns/0 ns typical (3.5 ns/0 ns worst case).

The AGP4X support uses CLK edges to log in both the CLK synchronous and source synchronous signals. The source synchronous signals can be shifted in time with respect to the CLK according to the AGP specifications. Therefore, the D_AD_STB or the D_SB_STB may not be stable within the Setup/Hold time period required by the logic analyzer with respect to the rising or falling AGP CLK edge. This may cause a Setup/Hold violation in the logic analyzer.

The signal D_AD_STB is a derived signal which is used to do the Setup/Hold adjustment of the D_AD_Strobe, AGP_Data_Hi, AGP_Data_Lo, BE_Hi and BE_Lo groups. The D_AD_STB signal is in the D_AD_Strobe group.

Similarly, the signal D_SB_STB is a derived signal which is used to do the Setup/Hold adjustment of the D_SB_Strobe, SBA_Hi and SBA_Lo groups. The D_SB_STB signal is in the D_SB_Strobe group.

Follow all steps, review the case studies and Figures 2–1 through 2–4 to determine if the Setup/Hold adjustments are required. You may also want to review the previous Setup/Hold statements.

1. Check that your graphics card is programmed for 4X mode.

2. Start a looping graphics program.
3. Load the AGP4X software from the disk to the logic analyzer.
4. To load the AGP4X support package from the logic analyzer System window, select the File menu > Load Support Package.
5. From the Load Support Package window, select AGP4X, select load, and then select Yes.

Setup MagniVu. Follow these steps to set up a MagniVu window:

1. From the logic analyzer System window, select the Window menu > New Data Window.
2. From the New Data Window, select Waveform, select Next, select AGP4X MagniVu, and then select Next.
3. Select finish. The New Data Window disappears and a waveform window is displayed.

Set Up the Trigger. Follow these steps to set up the Trigger to capture the D_AD_STB signal:

1. Select the System window, and then select Trig.
2. From the Trigger: AGP4X window, select If and fill in the four displayed fields with the following information.

First field	Channel
Second field	AD_STB_0
Third field	=
Fourth field	Low

3. Select OK.
4. Select the Waveform window, and then select Run. Wait for the TLA to capture and display the D_AD_STB waveform.

Consider the following case:

In Figure 2–1, the D_AD_STB signal has sufficient Setup/Hold time with respect to the CLK edge. In this case, no adjustment is required.

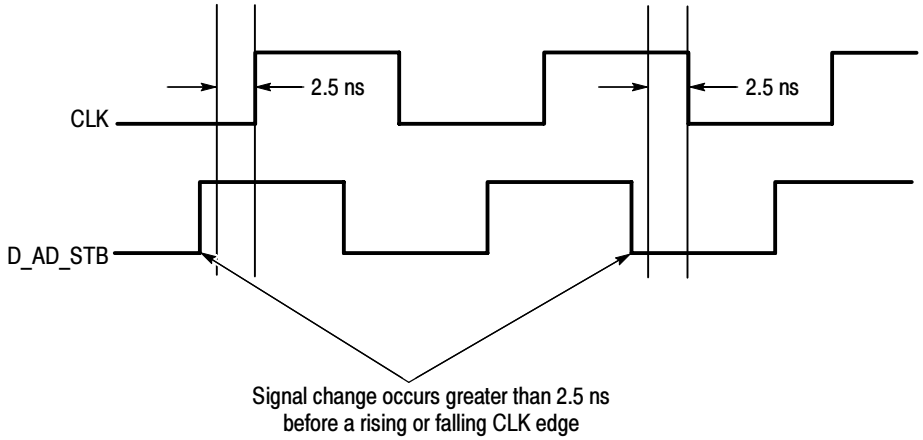


Figure 2–1: Examples of sufficient setup/hold times

Consider the next case:

In Figure 2–4, the D_AD_STB signal is changing within 2.5 ns of the CLK edge. You will need to modify the default Setup/Hold values by following these steps:

1. In the System window, click Setup. In the Setup:AGP4X window, click More (see Figure 2–2).

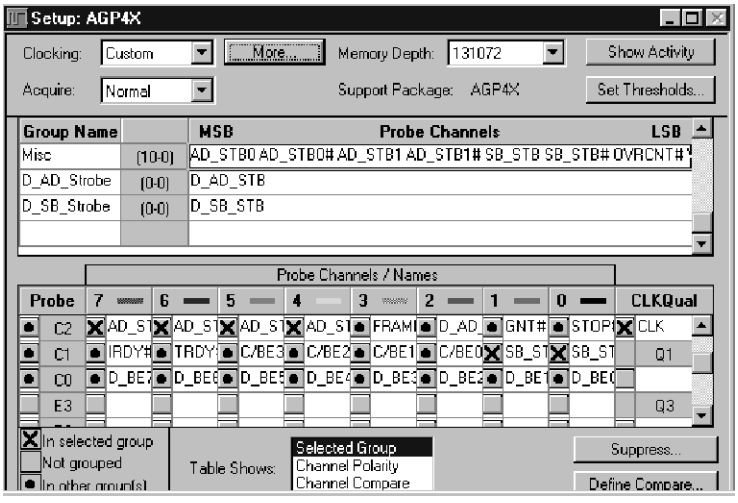


Figure 2–2: Setup:AGP4X window

2. In the Custom Options window, under the Setup/Hold Window, scroll down and click on the Support Package Default heading for D_AD_Strobe.

3. Select –500 ps/2.5 ns. Click OK (see Figure 2–3).

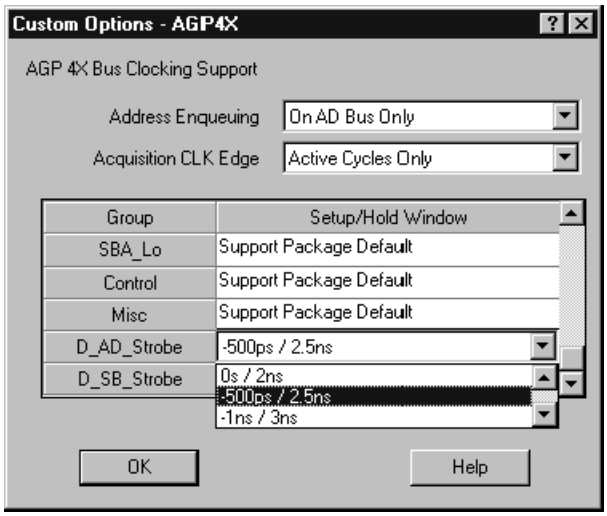


Figure 2–3: Custom option window

In this case, the Setup/Hold value is –0.5 ns Setup/2.5ns Hold. Each case may require different values. Be sure to select Setup/Hold values that are not violated by D_AD_STB.

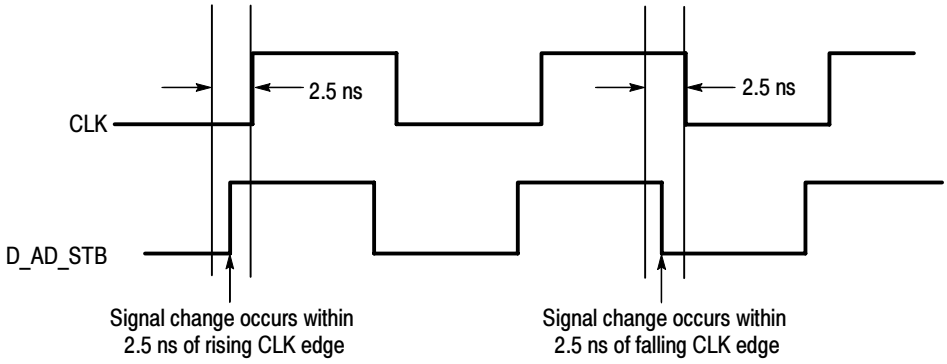


Figure 2–4: Setup/hold time violation examples

Once the Setup/Hold values for the D_AD_STB signal (that is, the D_AD_Strobe group) are determined, the same values must be entered in the AGP_Data_Hi, AGP_Data_Lo, BE_Hi and BE_Lo groups.

***NOTE**. Since the AD_STB timings with respect to CLK can be different for READs and WRITEs, the Setup/Hold time should satisfy the condition in both cases so that data can be accurately logged for AGP READs and AGP WRITEs.*

Similarly, the Setup/Hold values for the D_SB_STB signal (that is, D_SB_Strobe group) are determined and the same values are to be entered in the SBA_Hi and SBA_Lo groups.

Signals Not On the Probe Adapter

The TMS 808 probe adapter provides access for all of the AGP4X signals.

Extra Channels

The following channels on the logic analyzer are left free for you to connect to other signals of interest:

- Hi_E3:7-0 (for 136 channel module only)
- Hi_E2:7-0 (for 136 channel module only)
- Hi_E1:7-0 (for 136 channel module only)
- Hi_E0:7-0 (for 136 channel module only)
- Hi_C3:7-0
- Hi_C1:7-0
- Hi_C0:7-0
- Hi_A1:1-0

Specifications

Specifications

This chapter contains information regarding the specifications of the support.

Circuit Description

AGP4X support uses two distinctive types of transactions on the same physical bus, depending on which of the signals the transaction is synchronized to. The first set is synchronized to the 66 MHz AGP clock, and the second set is synchronized to the strobe signals. The timing relationship of the Strobe signals to the Clock is described in detail in the *Accelerated Graphics Port Interface Specification, Intel, Version 2.0, 1998*.

The AGP bus is a point to point bus and its behavior with an added third load is not specifified. If a third load (like the probe adapter) is added, it is the responsibility of the user to ensure that the system meets the AGP Interface specifications. The loading information and equivalent circuits for the probe adapter is provided on page 3–6. The critical timing constraints are mainly in the form of skew budget, which are separately allocated for the motherboard and the AGP4X connector.

The interface point between the motherboard and the AGP4X connector comes on the transmission line of the signals. So when probing the signals at the connector, you will encounter a composite signal made of the ongoing transmission and the reflection from the receiving end, as the AGP bus is source terminated. As the signaling period reduces and approaches the transit time over the bus length, it becomes very difficult to extract valid data from the composite waveform. In the case of TMS 808 support, circuitry on the extender board performs the task of extracting digital signals from the composite wave present on the bus.

Once the digital signals are extracted, the transactions need to be captured by the Logic Analyzer. The two issues involved are a high data rate (266 MHz), that is more than the logic analyzer module can handle and two types of synchronization, as mentioned previously.

The first issue, high data rate, is handled by demultiplexing the data, reducing the rate to 133 MHz. At this rate, the logic analyzer is able to directly acquire the data presented. The respective Strobe signals are used to latch data in latches, and both edges of the AGP clock are used to log these latched outputs.

The second issue, two types of synchronization, are shown in the block diagram of the logic circuit, which implements demultiplexing the data (see Figure 3–1).

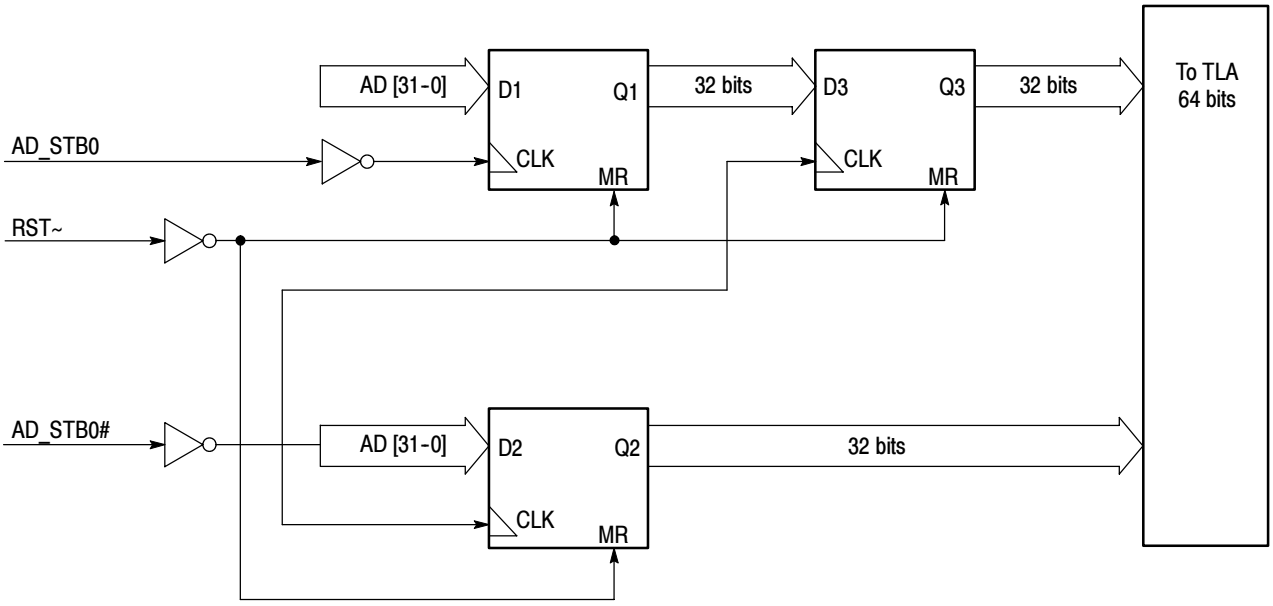


Figure 3-1: Block diagram for AD bus

The first data value on the 32-bit bus is latched into latch D1 by the falling edge of AD_STB0. In fact, the lower significant 16 bits uses AD_STB0 and the upper significant 16 bits uses AD_STB1, but for simplicity, the block diagram shows only a single 32 bit latch. The falling edge of the complementary strobe AD_STB0# latches the second data in D2, at the same time moving the data at the output of D1 into another latch D3. This is done to avoid the D1 data being overwritten by the next edge of the AD_STB0. More than three strobe edges cannot be accommodated in one half cycle of AGP clock, so the TLA always gets a chance to acquire the data before it gets overwritten. When lower speed (1X, PCI for example) cycles are being run, TLA picks up the AD bus information directly from the bus rather than from the latched output. On the user interface, the latched AD bus data appears as AGP_Data_Hi and AGP_Data_Lo.

The same principle is applied on the side band signals, using another set of latches (see Figure 3-2).

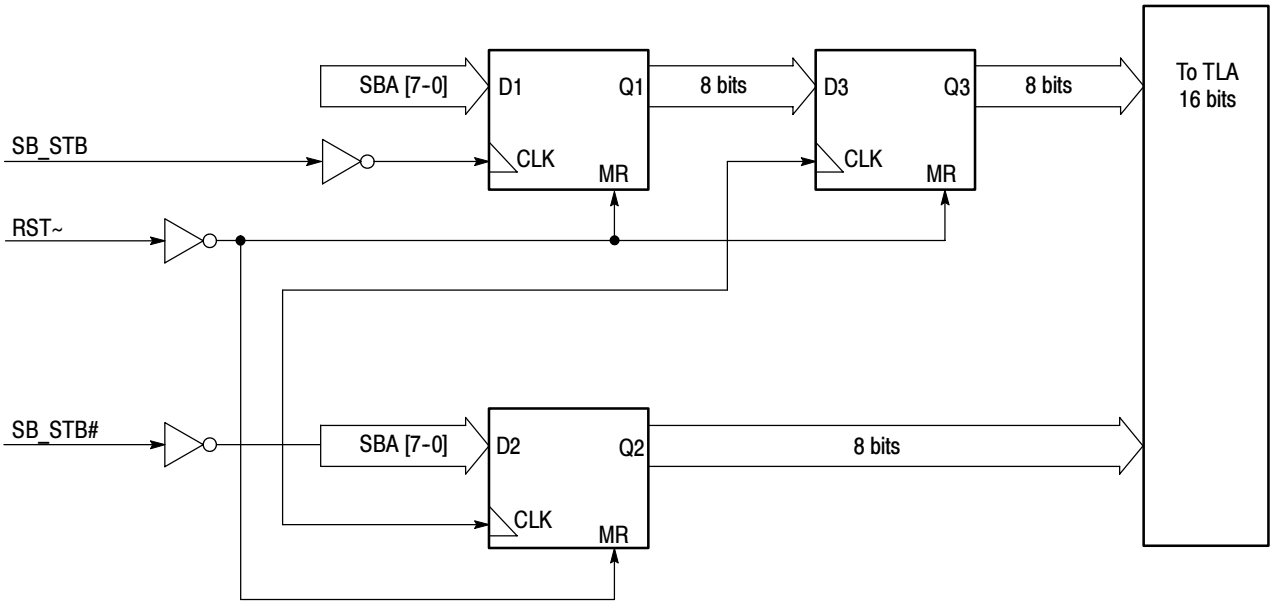


Figure 3-2: Block diagram for the SBA bus

The 32-bit AD bus splits into a 64-bit bus at the logic analyzer input, and the 8-bit SBA bus splits into 16 bits. After this, latched data is valid up to 7.5 ns, in most cases it will provide the necessary setup time for the logic analyzer, even if the AGP clock is used for logging in data. In rare instances, the clock-edge-to-strobe timing may have a setup/hold violation in the logic analyzer. In this case, the adjustable Setup/Hold values of the logic analyzer can be used to make accurate data acquisitions.

For the logic analyzer to detect the availability of fresh data, a qualifier is required that can be reliably acquired at the same acquisition speed. Since no signal from the AGP bus can be used for this purpose, two signals are derived from the strobe. A single-toggle flip-flop is used to generate the common qualifier D_AD_STB. Data is always logged in as 64 bits into the logic analyzer. Only when the second set of data arrives on the falling edge of the AD_STB0#, is the data logged in as 64 bits. Also, the support makes use of the fact that there are always 4 falling edges occurring in the AGP4x; irrespective, of whether the data is valid or not. Similarly another qualifier is derived for the SBA signals (see Figure 3-3).

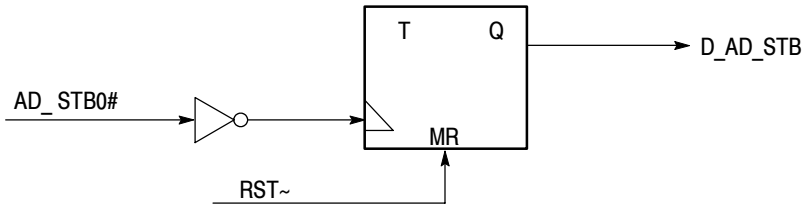


Figure 3-3: Qualifier generation

The AGP 2X support included with this package operates in a similar manner. The only difference is that the derived qualifiers get replaced by the corresponding strobe signals themselves.

The support masters all signals in all three cases; when an AGP transfer is on the AD bus, there is activity on the side band strobes, and the system is running PCI cycles. This means, except for the bus whose activity caused the master point, other buses may have invalid data. The disassembler locates such invalid data on the various buses and marks them as invalid with dashes. In the SBA mode, the side band strobe is active even when there is no data to be passed. So, if the data being queued is NOPs, and there is no valid data on any other buses, such samples are suppressed by the disassembler.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a System Under Test (SUT). Table 3-1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

Table 3-1: Electrical specifications

Characteristics	Requirements
SUT DC power requirements	The support uses an external power supply and does not draw any current from the SUT.
Probe adapter: DC power requirements	
Voltage, VCC	4.75 – 5.25 VDC
Current, VCC	$I_{typical}$ 4.0 A

Table 3-1: Electrical specifications (cont.)

Characteristics	Requirements
	$I_{maximum}$ 4.2 A
AC adapter	
Input Voltage rating	90 - 265 V CAT II
Input Frequency Rating	47 - 63 Hz
Output Voltage Rating	5 V
Output Current Rating	8 A
Output Power Rating	40 W
SUT clock rate	Maximum 66 MHz
Set up and hold time requirements	SUT should meet AGP 2.0 specifications
Note; *All Reserved pins are connected through the probe adapter. All VCC3.3 pins are shorted together on the probe adapter. All Vddq3.3 pins are shorted together on the probe adapter. All 5.0 V pins are shorted together on the probe adapter.*	

Table 3-2 shows the environmental specifications.

Table 3-2: Environmental specifications[1]

Characteristic	Description
Temperature	
Maximum operating	+50 °C (+122 °F)[2]
Minimum operating	0 °C (+32 °F)
Non operating	-55 °C to +75 °C (-67 ° to +167 °F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

1 Designed to meet Tektronix standard 062-2847-00 class 5.

2 Not to exceed AGP4X bus thermal considerations. Forced air cooling might be required.

Loading and Equivalent Circuits

The load presented to the SUT by the AGP probe adapter is low. The following approximation of the probe adapter loading is sufficient for most circuit-simulation calculations.

Table 3–3 shows the values you can use to calculate characteristics of the lossy delay lines shown in Figure 3–4 on page 3–7.

Table 3–3: Lossy delay line values

Characteristic	Value
C (capacitance)	3 pF per inch
L (inductance)	10.8 nH per inch
R (resistance)	.067 Ω per inch
Z_0 (impedance)	60 Ω

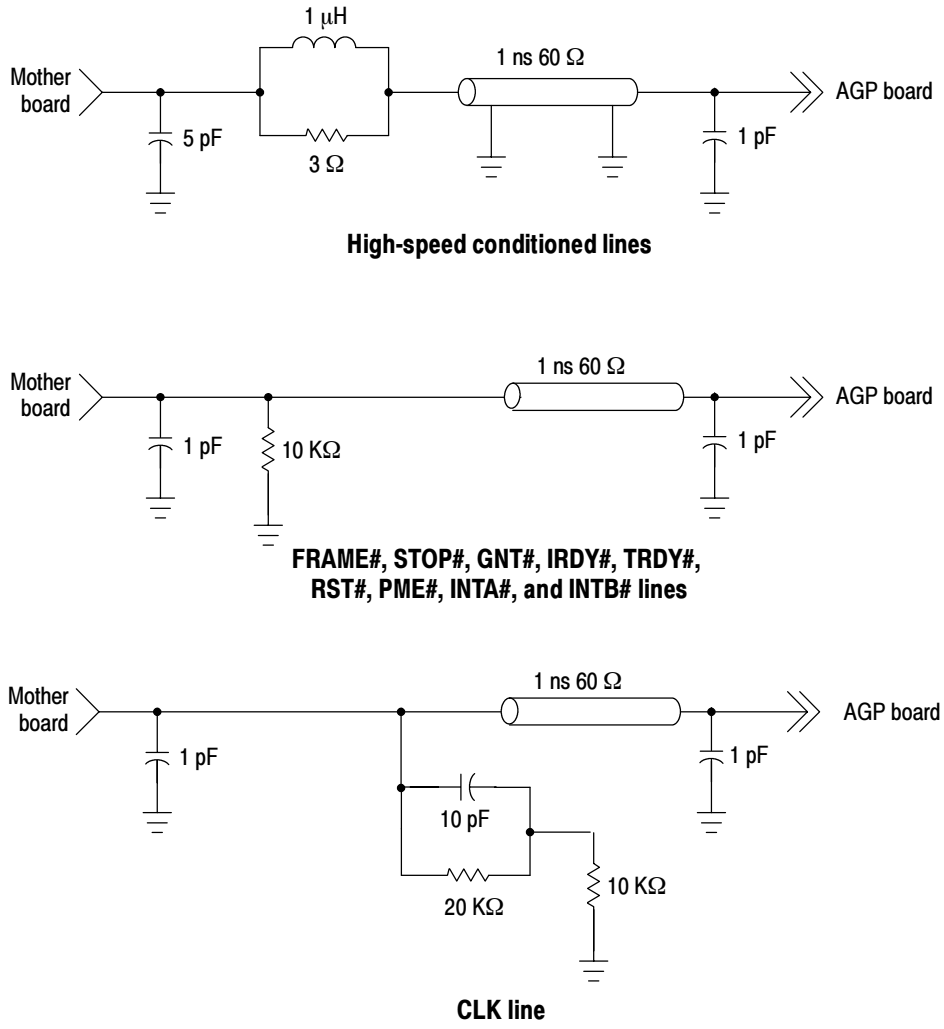


Figure 3-4: Equivalent circuit loads for the probe adapter

Figure 3-5 shows the dimensions of the probe adapter.

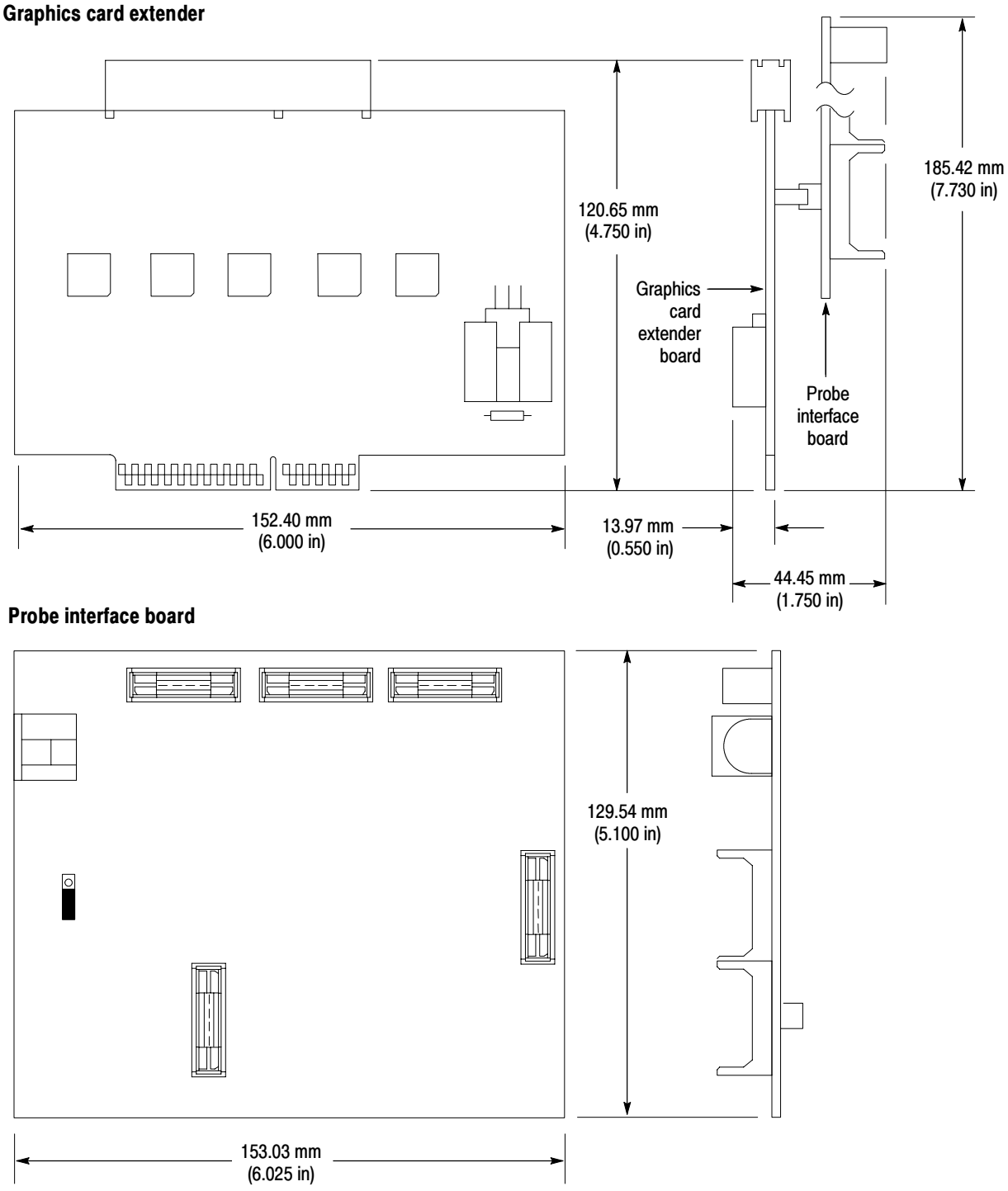


Figure 3-5: Probe adapter dimensions

Diagrams

Diagrams and Circuit Board Illustrations

This section contains the troubleshooting procedures, block diagrams, circuit board illustrations, component locator tables, waveform illustrations, and schematic diagrams.

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975. Abbreviations are based on ANSI Y1.1-1972.

Logic symbology is based on ANSI/IEEE Standard 91-1984 in terms of positive logic. Logic symbols depict the logic function performed and can differ from the manufacturer's data.

The tilde (~) preceding a signal name indicates that the signal performs its intended function when in the low state.

Other standards used in the preparation of diagrams by Tektronix, Inc., include the following:

- Tektronix Standard 062-2476 Symbols and Practices for Schematic Drafting
- ANSI Y14.159-1971 Interconnection Diagrams
- ANSI Y32.16-1975 Reference Designations for Electronic Equipment
- MIL-HDBK-63038-1A Military Standard Technical Manual Writing Handbook

Component Values

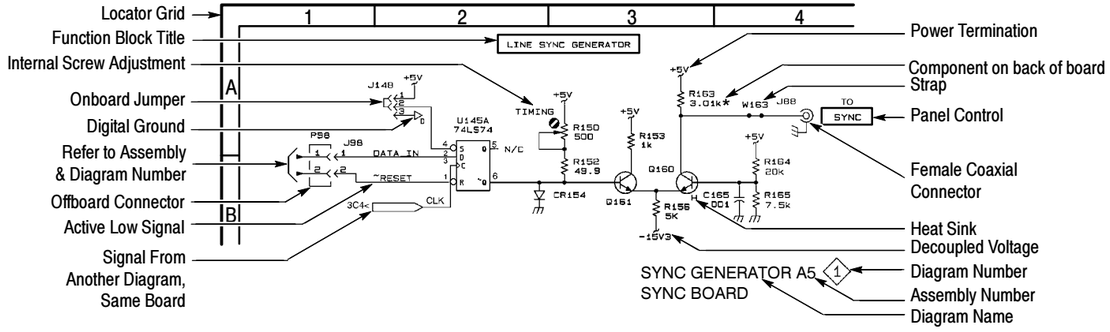
Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors: Values one or greater are in picofarads (pF).
Values less than one are in microfarads (µF).

Resistors: Values are in Ohms (Ω).

Graphic Items and Special Symbols Used in This Manual

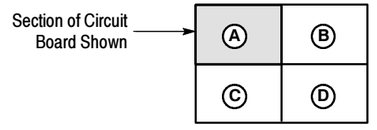
Each assembly in the instrument is assigned an assembly number (for example A5). The assembly number appears in the title on the diagram, in the lookup table for the schematic diagram, and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assembly in numerical sequence; the components are listed by component number.

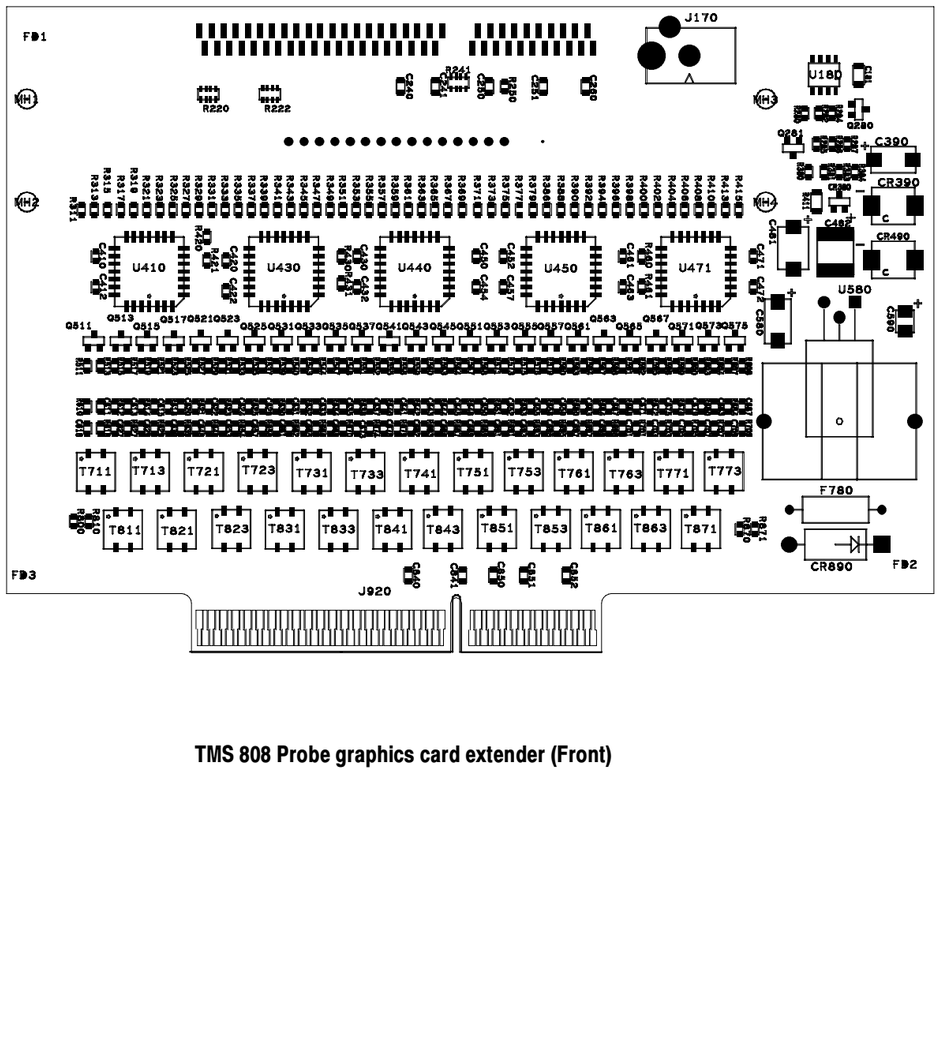


Component Locator Diagrams

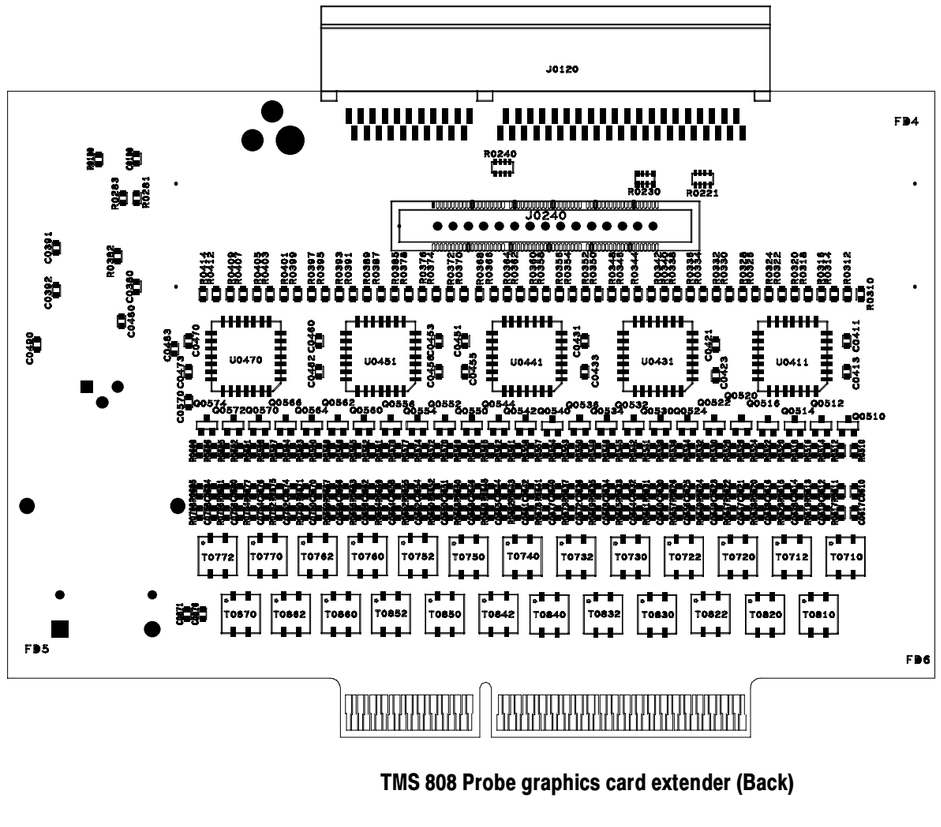
The schematic diagram and circuit board component location illustrations have grids marked on them. The component lookup tables refer to these grids to help you locate a component. The circuit board illustration appears only once; its lookup table lists the diagram number of all diagrams on which the circuitry appears.

Some of the circuit board component location illustrations are expanded and divided into several parts to make it easier for you to locate small components. To determine which part of the whole locator diagram you are looking at, refer to the small locator key shown below. The gray block, within the larger circuit board outline, shows where that part fits in the whole locator diagram. Each part in the key is labeled with an identifying letter that appears in the figure titles under component locator diagrams.

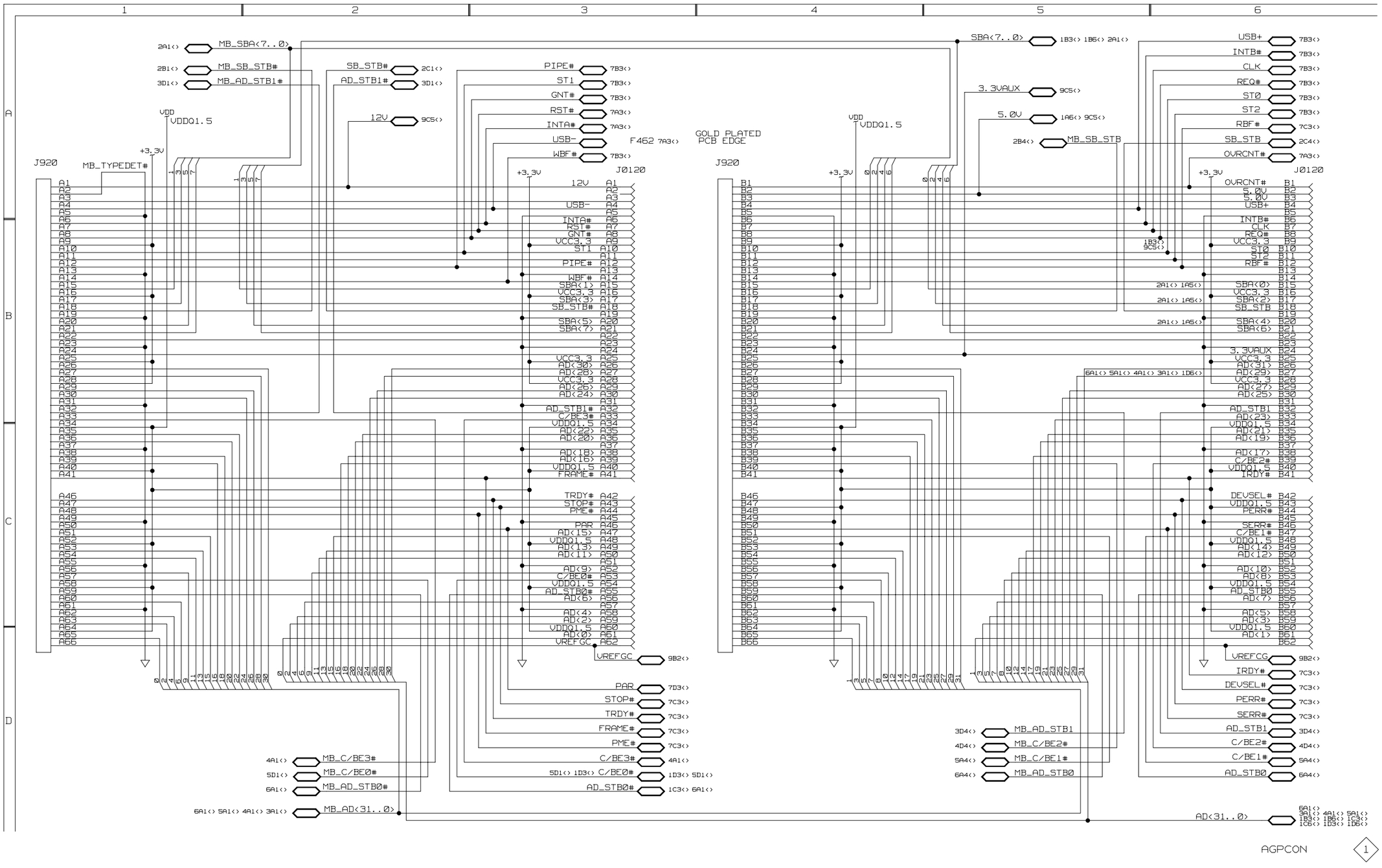


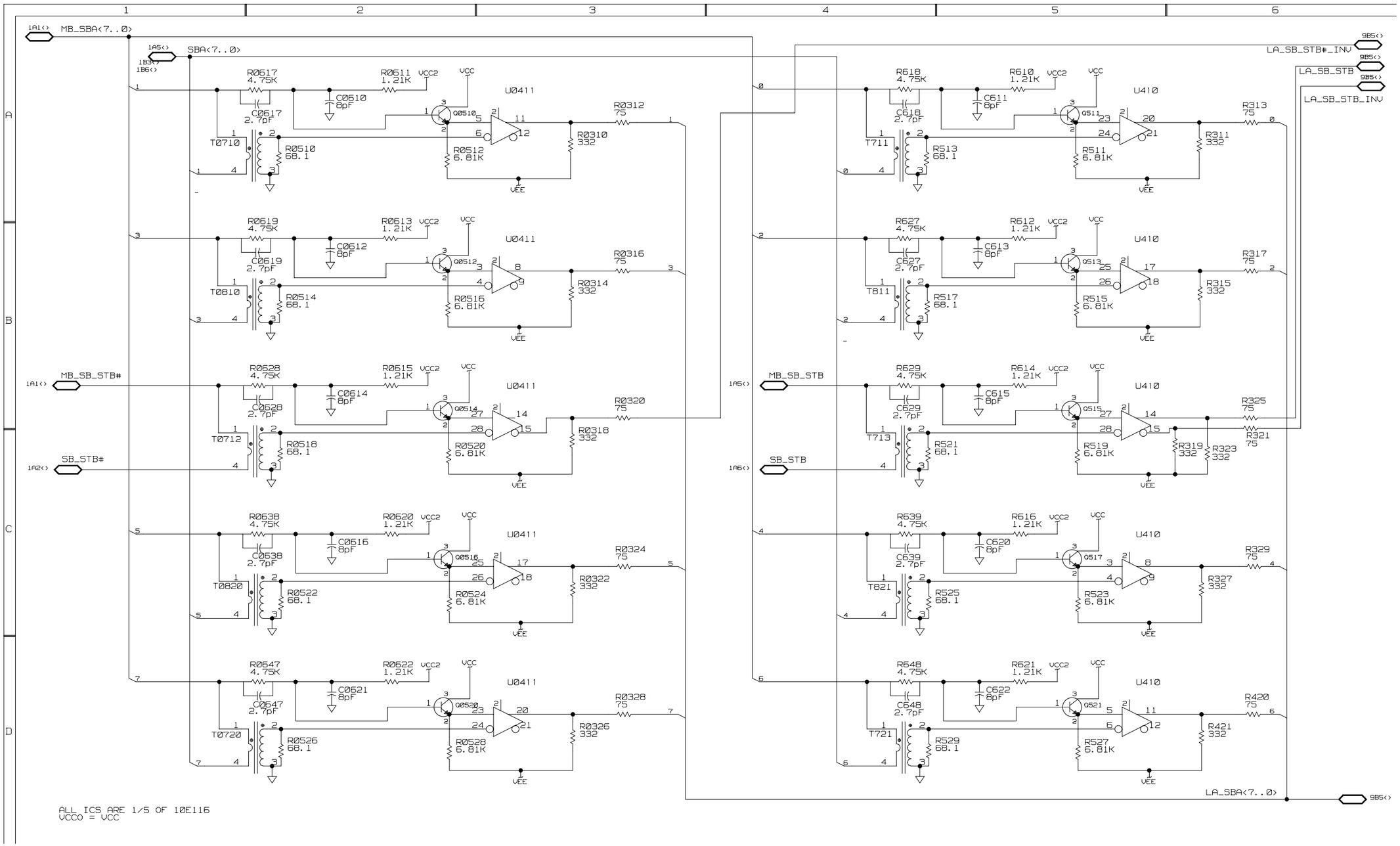


TMS 808 Probe graphics card extender (Front)

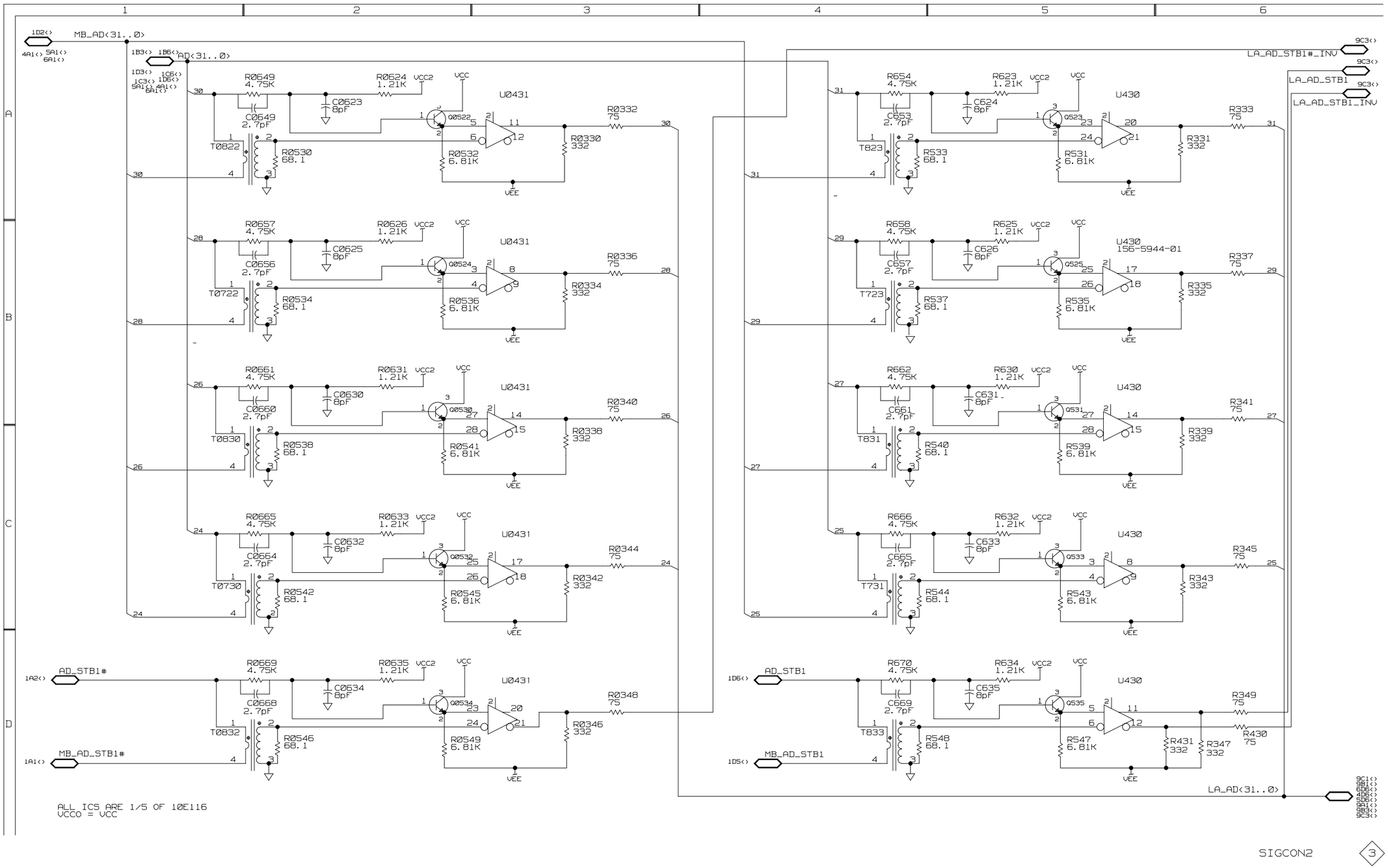


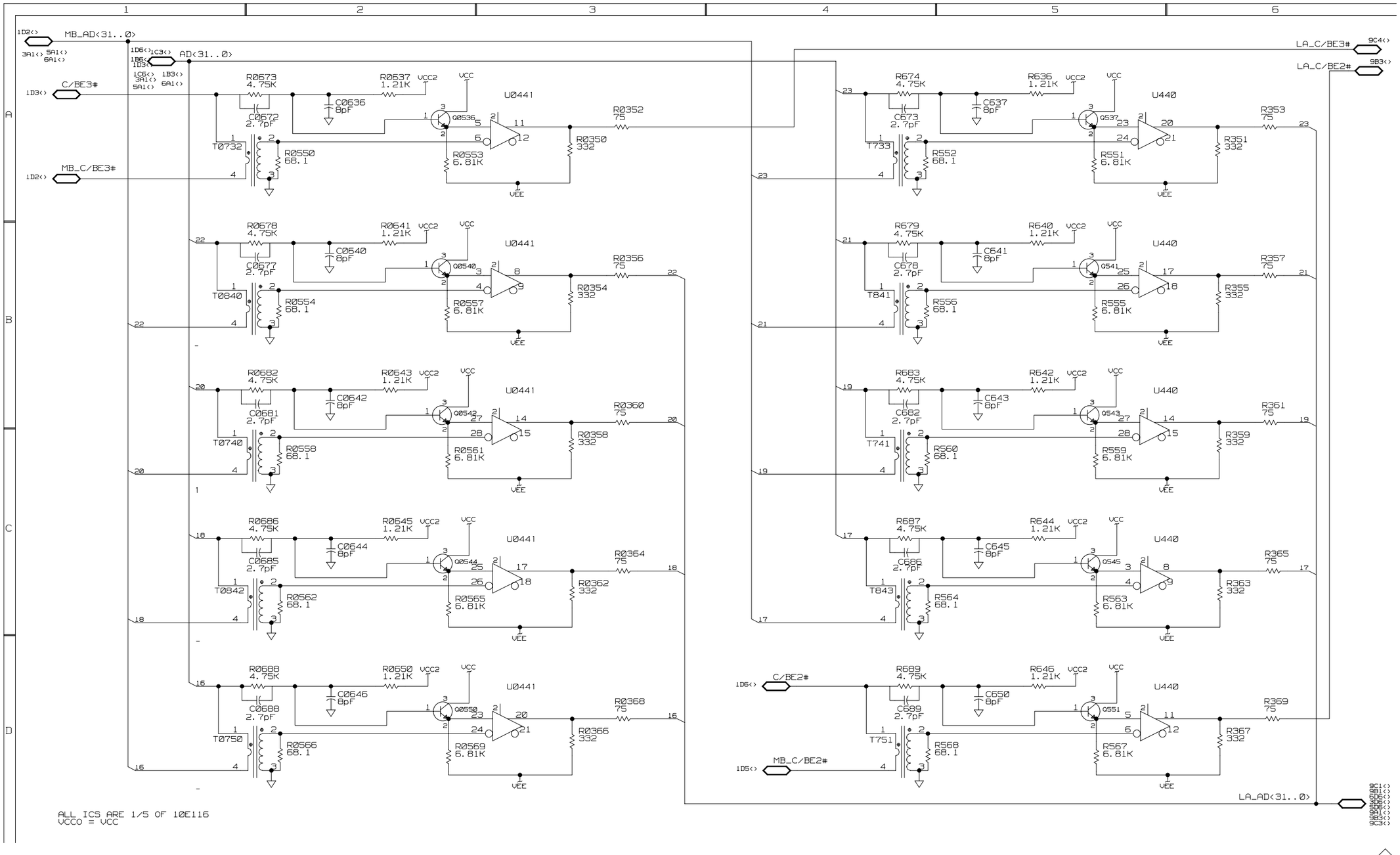
TMS 808 Probe graphics card extender (Back)


MB_SBA<7..0>
MB_SB_STB#
MB_AD_STB1#
SB_STB#
AD_STB1#
12V
PIPE#
ST1
GNT#
RST#
INTA#
USB-
WBF#
F462
GOLD PLATED PCB EDGE
SBA<7..0>
3.3VAUX
5.0V
MB_SB_STB
USB+
INTB#
CLK
REQ#
ST0
ST2
RBF#
SB_STB
OVRCNT#
VDD
VDDQ1.5
+3.3V
J920
J0120
MB_TYPEDET#
VREFGC
PAR
STOP#
TRDY#
FRAME#
PME#
C/BE3#
C/BE0#
AD_STB0#
MB_C/BE3#
MB_C/BE0#
MB_AD_STB0#
MB_AD<31..0>
MB_AD_STB1
MB_C/BE2#
MB_C/BE1#
MB_AD_STB0
AD<31..0>
AGPCON


MB_SBA<7..0>
SBA<7..0>
LA_SB_STB#_INV
LA_SB_STB
LA_SB_STB_INV
MB_SB_STB#
SB_STB#
MB_SB_STB
SB_STB
LA_SBA<7..0>
U0411
U410
VCC
VCC2
VEE
ALL ICS ARE 1/5 OF 10E116
VCCO = VCC

SIGCON1 2


MB_AD<31..0>
AD<31..0>
LA_AD_STB1#_INV
LA_AD_STB1
LA_AD_STB1_INV
AD_STB1#
MB_AD_STB1#
AD_STB1
MB_AD_STB1
LA_AD<31..0>
U0431
U430
U430 156-5944-01
VCC
VCC2
VEE
ALL ICS ARE 1/5 OF 10E116
VCCO = VCC
SIGCON2
3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MB_C/BE3#
LA_C/BE3#
LA_C/BE2#
C/BE2#
MB_C/BE2#
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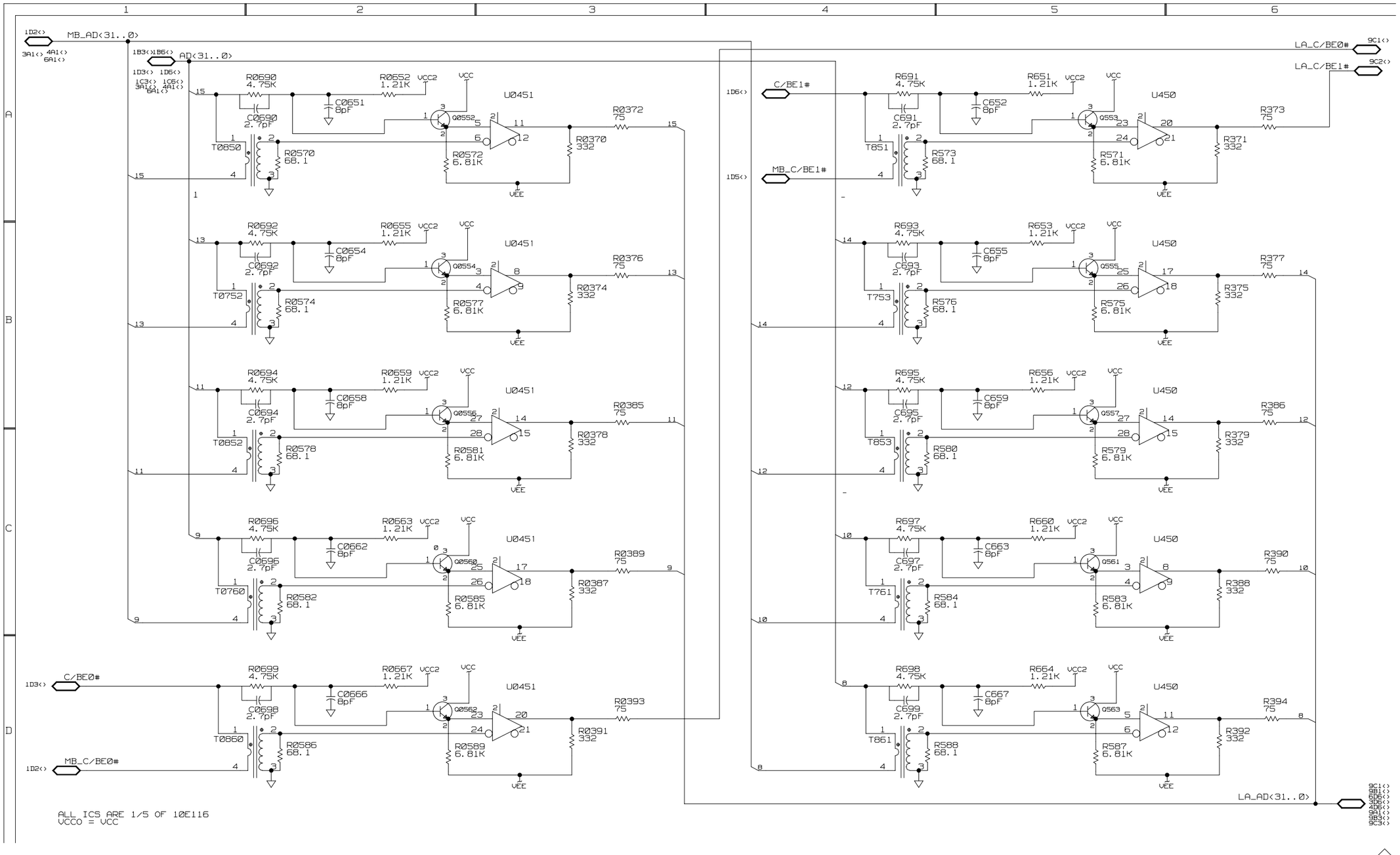
U440
R0673 4.75K
R0637 1.21K
C0636 8pF
C0672 2.7pF
T0732
R0550 68.1
R0553 6.81K
R0352 75
R0350 332
R0678 4.75K
R0641 1.21K
C0640 8pF
C0677 2.7pF
T0840
R0554 68.1
R0557 6.81K
R0356 75
R0354 332
R0682 4.75K
R0643 1.21K
C0642 8pF
C0681 2.7pF
T0740
R0558 68.1
R0561 6.81K
R0360 75
R0358 332
R0686 4.75K
R0645 1.21K
C0644 8pF
C0685 2.7pF
T0842
R0562 68.1
R0565 6.81K
R0364 75
R0362 332
R0688 4.75K
R0650 1.21K
C0646 8pF
C0688 2.7pF
T0750
R0566 68.1
R0569 6.81K
R0368 75
R0366 332
R674 4.75K
R636 1.21K
C637 8pF
C673 2.7pF
T733
R552 68.1
R551 6.81K
R353 75
R351 332
R679 4.75K
R640 1.21K
C641 8pF
C678 2.7pF
T841
R556 68.1
R555 6.81K
R357 75
R355 332
R683 4.75K
R642 1.21K
C643 8pF
C682 2.7pF
T741
R560 68.1
R559 6.81K
R361 75
R359 332
R687 4.75K
R644 1.21K
C645 8pF
C686 2.7pF
T843
R564 68.1
R563 6.81K
R365 75
R363 332
R689 4.75K
R646 1.21K
C650 8pF
C689 2.7pF
T751
R568 68.1
R567 6.81K
R369 75
R367 332
VCC
VCC2
VEE
ALL ICS ARE 1/5 OF 10E116
VCCO = VCC
SIGCON3
4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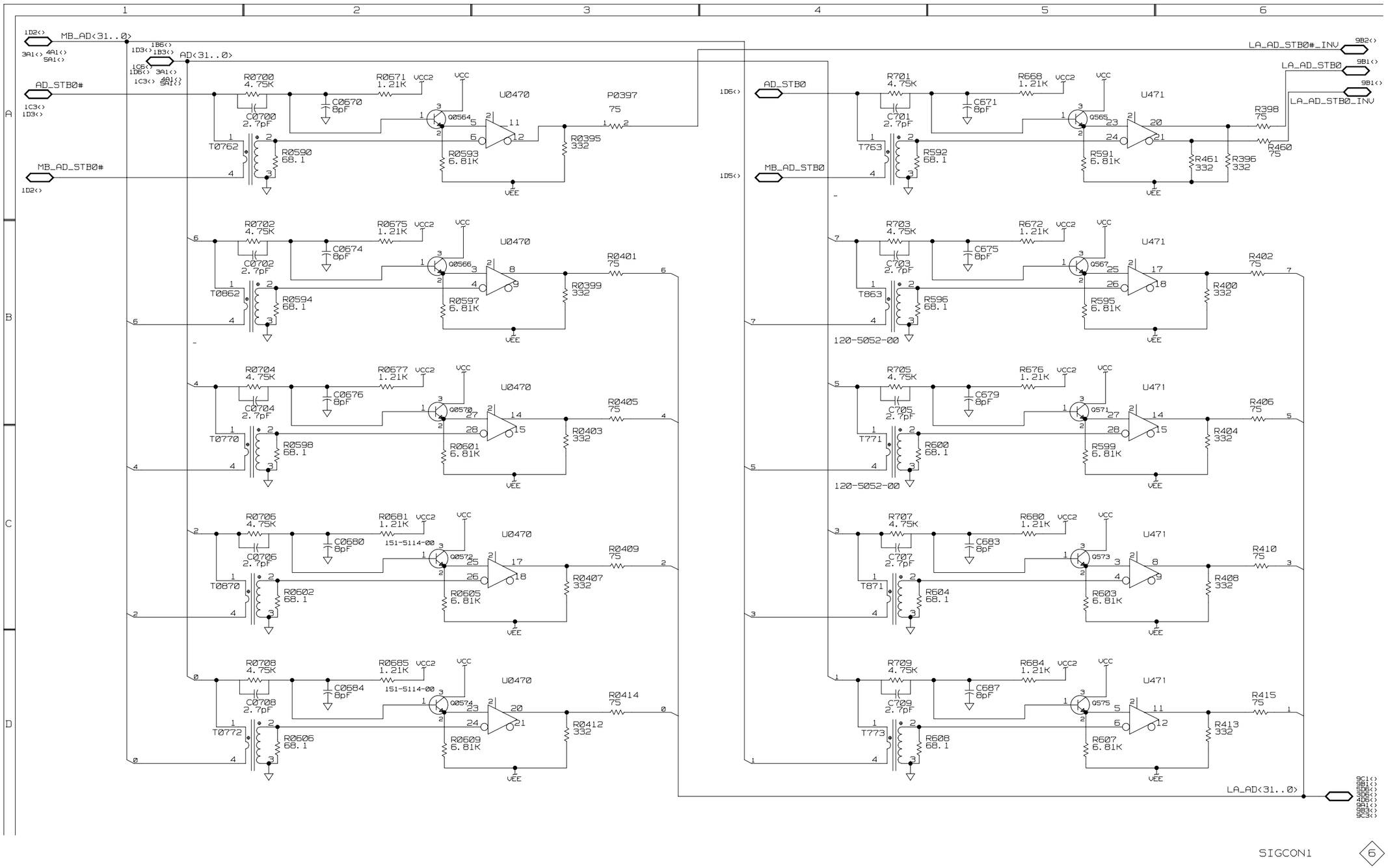
AD<31..0>
C/BE1#
MB_C/BE1#
LA_C/BE0#
LA_C/BE1#
C/BE0#
MB_C/BE0#
LA_AD<31..0>
U0451
U450
VCC
VCC2
VEE
ALL ICS ARE 1/5 OF 10E116
VCCO = VCC
SIGCON4
5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AD<31..0>
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MB_AD_STB0#
AD_STB0
MB_AD_STB0
LA_AD_STB0#_INV
LA_AD_STB0
LA_AD_STB0_INV
LA_AD<31..0>
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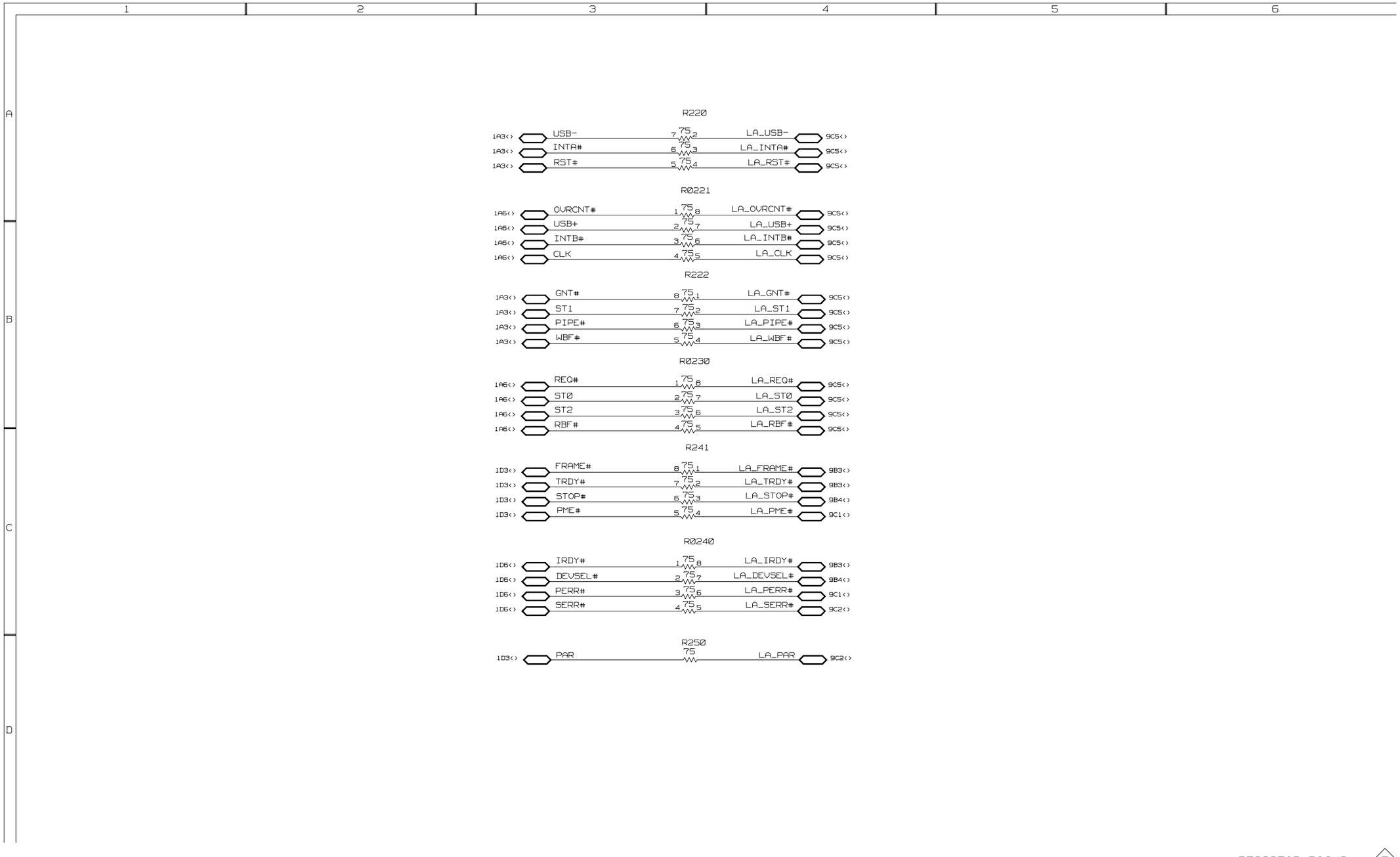
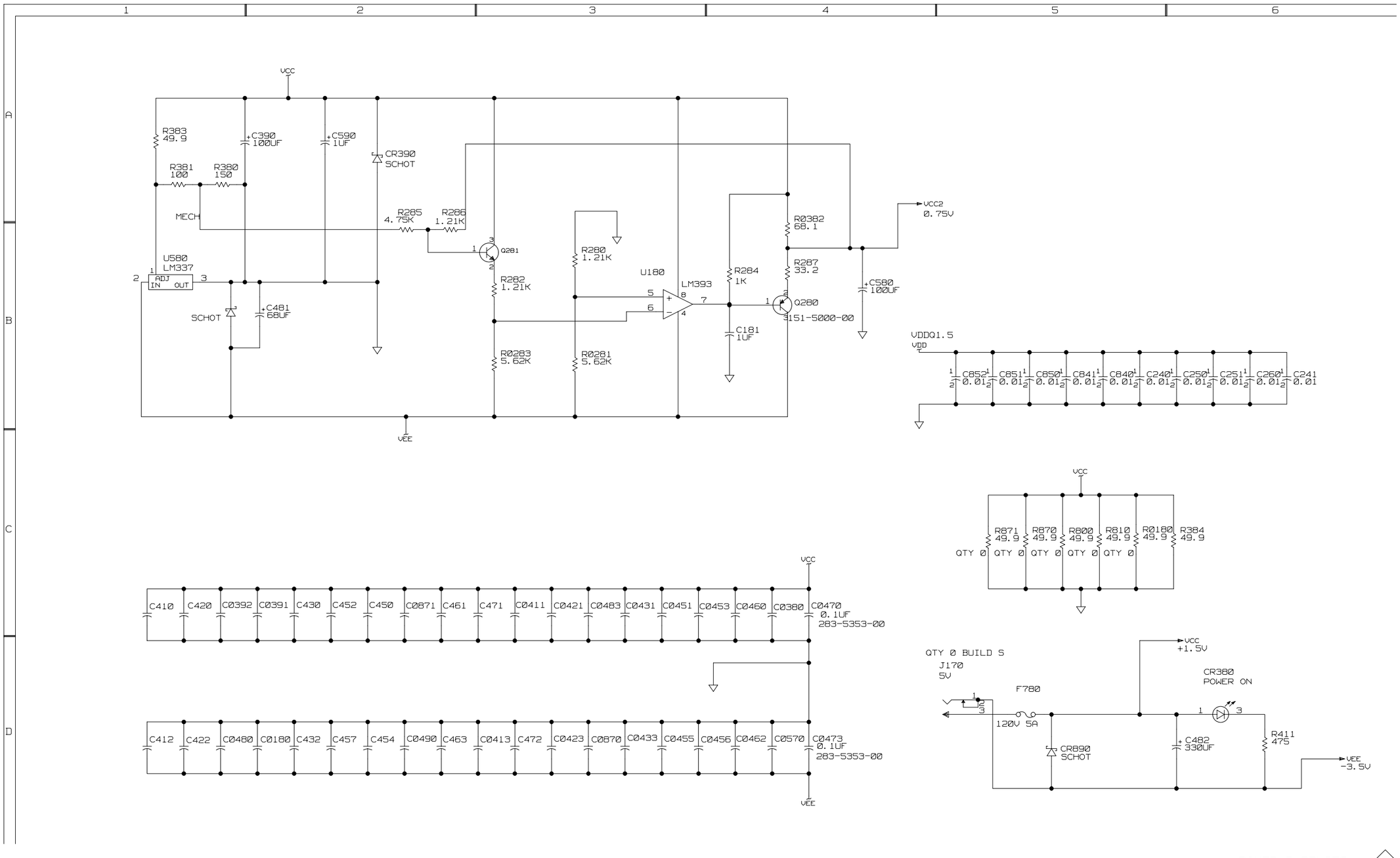
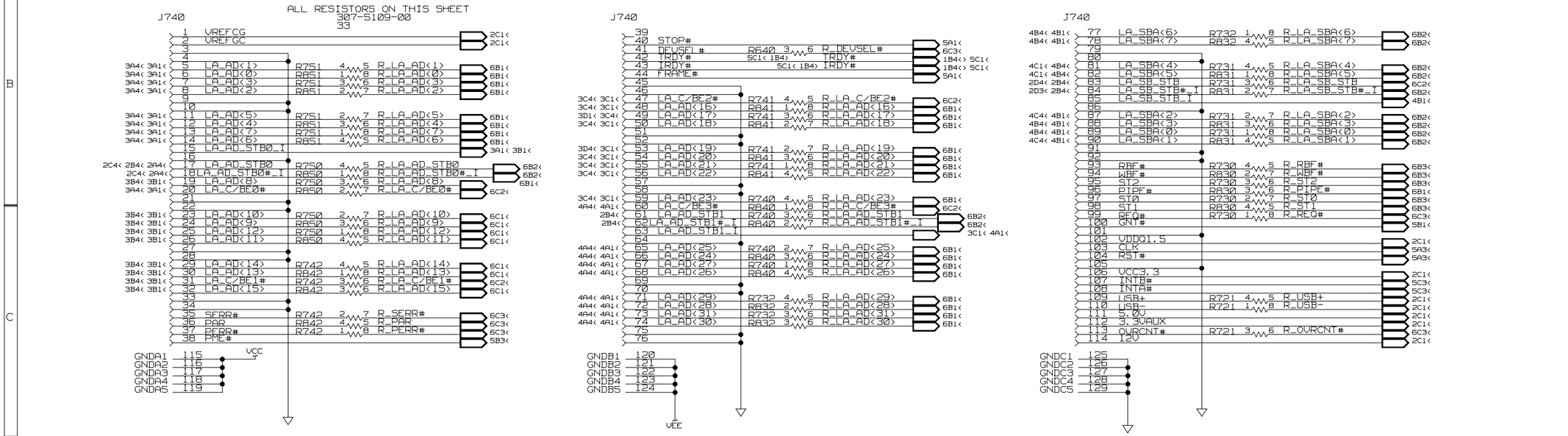
R0571 1.21K
C0700 2.7pF
C0670 8pF
U0470
Q0564
P0397 75
T0762
R0590 68.1
R0593 6.81K
R0395 332
VCC2
VCC
VEE
R0702 4.75K
R0575 1.21K
C0702 2.7pF
C0674 8pF
Q0566
R0401 75
T0862
R0594 68.1
R0597 6.81K
R0399 332
R0704 4.75K
R0577 1.21K
C0704 2.7pF
C0676 8pF
Q0570
R0405 75
T0770
R0598 68.1
R0601 6.81K
R0403 332
R0706 4.75K
R0581 1.21K
C0706 2.7pF
C0680 8pF
151-5114-00
Q0572
R0409 75
T0870
R0602 68.1
R0605 6.81K
R0407 332
R0708 4.75K
R0585 1.21K
C0708 2.7pF
C0684 8pF
Q0574
R0414 75
T0772
R0606 68.1
R0609 6.81K
R0412 332
R701 4.75K
R668 1.21K
C701 2.7pF
C671 8pF
U471
Q565
R398 75
T763
R592 68.1
R591 6.81K
R461 332
R396 332
R460 75
R703 4.75K
R672 1.21K
C703 2.7pF
C675 8pF
Q567
R402 75
T863
R596 68.1
R595 6.81K
R400 332
120-5052-00
R705 4.75K
R676 1.21K
C705 2.7pF
C679 8pF
Q571
R406 75
T771
R600 68.1
R599 6.81K
R404 332
R707 4.75K
R680 1.21K
C707 2.7pF
C683 8pF
Q573
R410 75
T871
R604 68.1
R603 6.81K
R408 332
R709 4.75K
R684 1.21K
C709 2.7pF
C687 8pF
Q575
R415 75
T773
R608 68.1
R607 6.81K
R413 332
SIGCON1
6



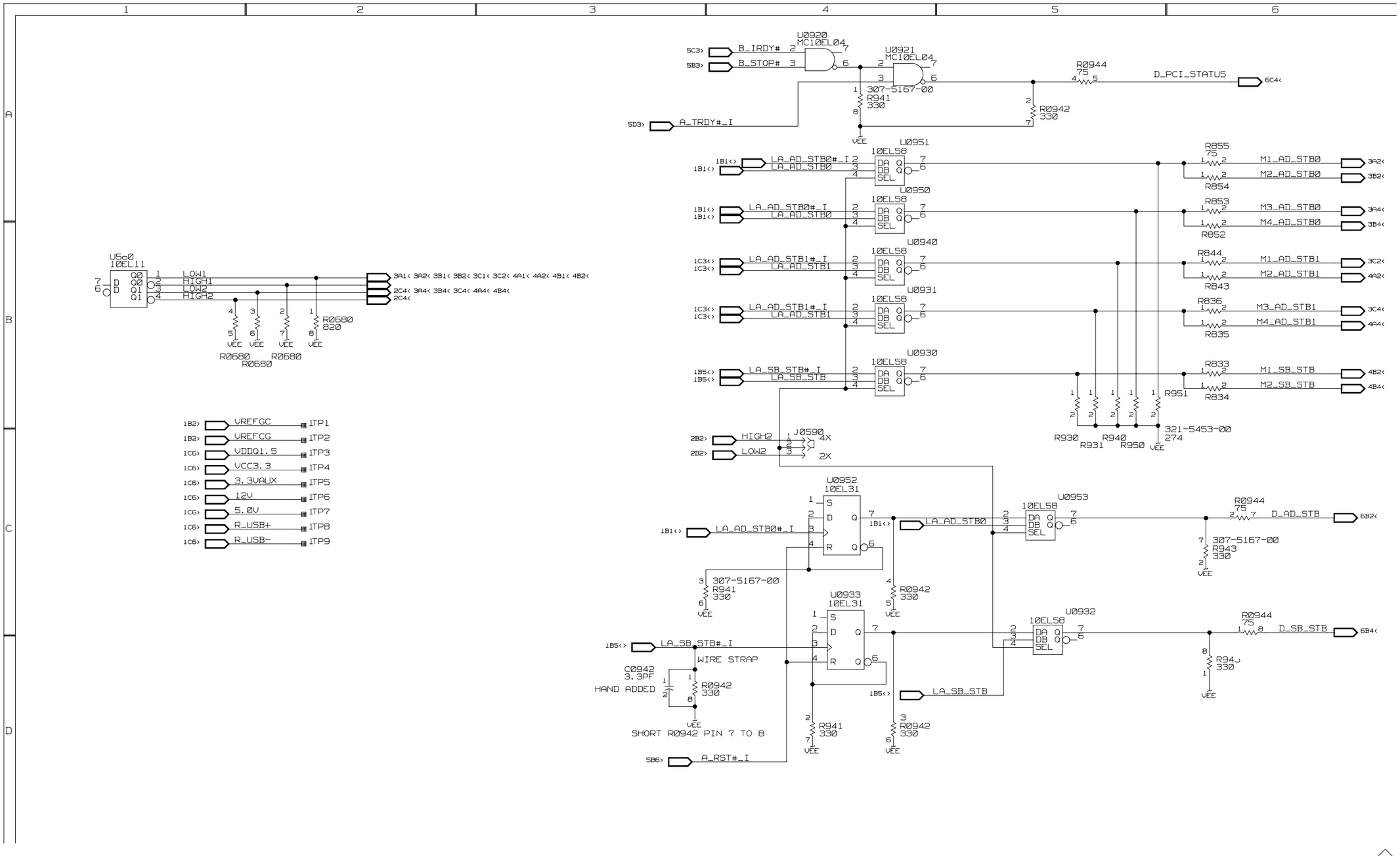
RESISTOR PACKS 7



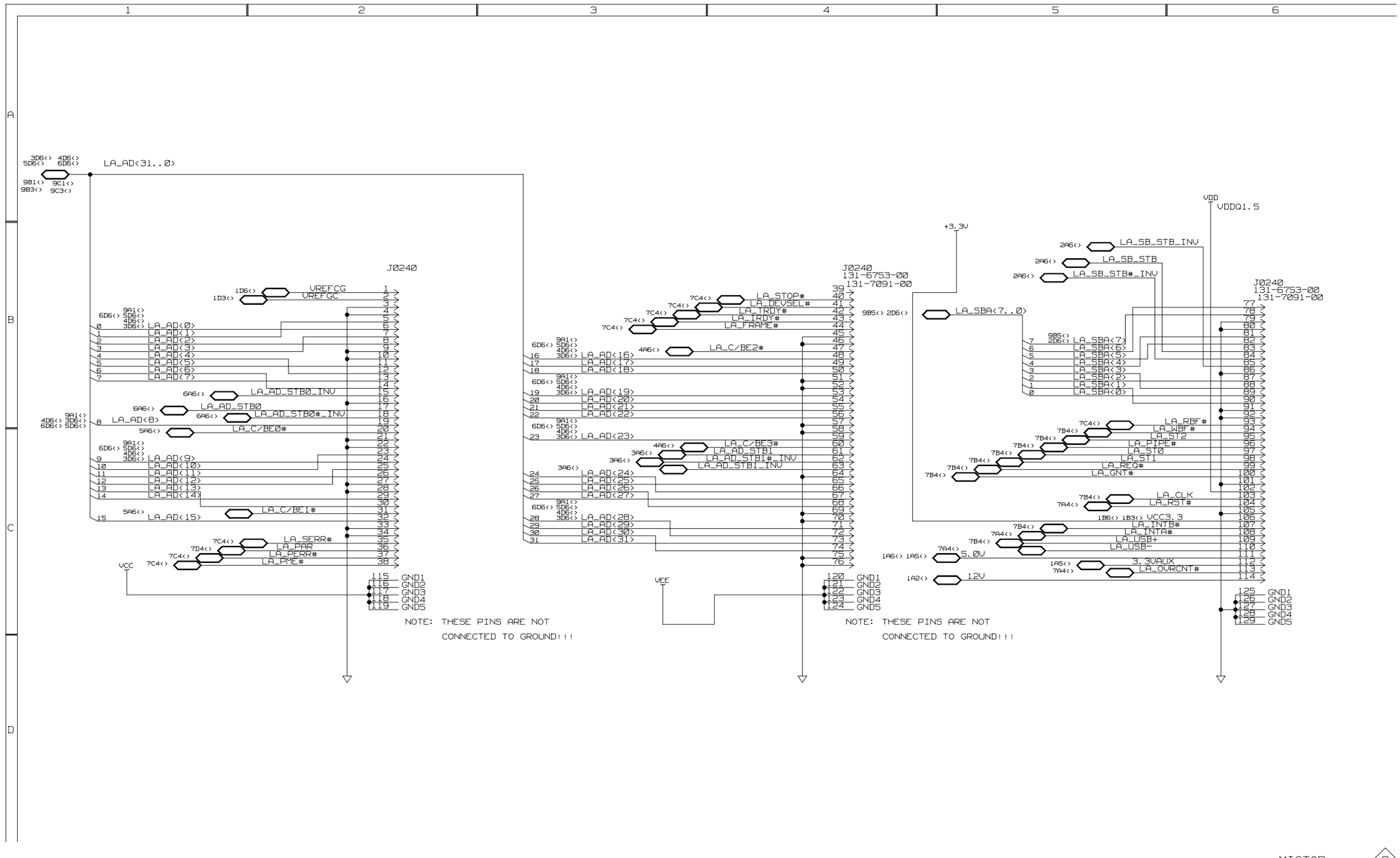
POWER SUPPLIES 8



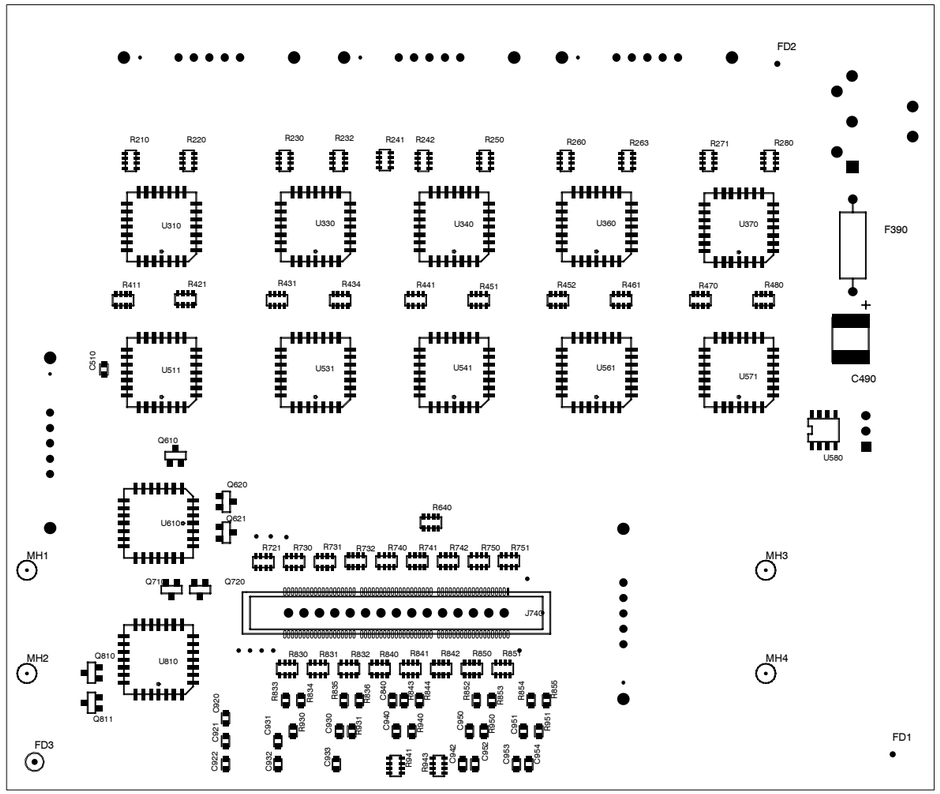
LONG_MICT_M A01 1


U5Ø
10EL11
LOW1
HIGH1
LOW2
HIGH2
3A1‹ 3A2‹ 3B1‹ 3B2‹ 3C1‹ 3C2‹ 4A1‹ 4A2‹ 4B1‹ 4B2‹
2C4‹ 3A4‹ 3B4‹ 3C4‹ 4A4‹ 4B4‹
2C4‹
R0680
820
R0680
R0680
R0680
VEE
1B2› VREFGC iTP1
1B2› VREFCG iTP2
1C6› VDDQ1.5 iTP3
1C6› VCC3.3 iTP4
1C6› 3.3VAUX iTP5
1C6› 12V iTP6
1C6› 5.0V iTP7
1C6› R_USB+ iTP8
1C6› R_USB- iTP9
U0920
MC10EL04
U0921
MC10EL04
5C3› B_IRDY#
5B3› B_STOP#
5D3› A_TRDY#_I
307-5167-00
R941
330
R0942
330
R0944
75
D_PCI_STATUS
6C4‹
VEE
U0951
10EL58
U0950
U0940
U0931
U0930
1B1‹› LA_AD_STB0#_I
LA_AD_STB0
1C3‹› LA_AD_STB1#_I
LA_AD_STB1
1B5‹› LA_SB_STB#_I
LA_SB_STB
DA Q
DB Q
SEL
R855
R854
R853
R852
R844
R843
R836
R835
R833
R834
M1_AD_STB0
M2_AD_STB0
M3_AD_STB0
M4_AD_STB0
M1_AD_STB1
M2_AD_STB1
M3_AD_STB1
M4_AD_STB1
M1_SB_STB
M2_SB_STB
3A2‹
3B2‹
3A4‹
3B4‹
3C2‹
4A2‹
3C4‹
4A4‹
4B2‹
4B4‹
R951
321-5453-00
274
R930
R931
R940
R950
2B2› HIGH2
2B2› LOW2
J0590
4X
2X
U0952
10EL31
U0953
U0933
U0932
S
D
R
Q
LA_AD_STB0
LA_SB_STB
R0944
D_AD_STB
D_SB_STB
6B2‹
6B4‹
WIRE STRAP
C0942
3.3PF
HAND ADDED
SHORT R0942 PIN 7 TO 8
5B6› A_RST#_I

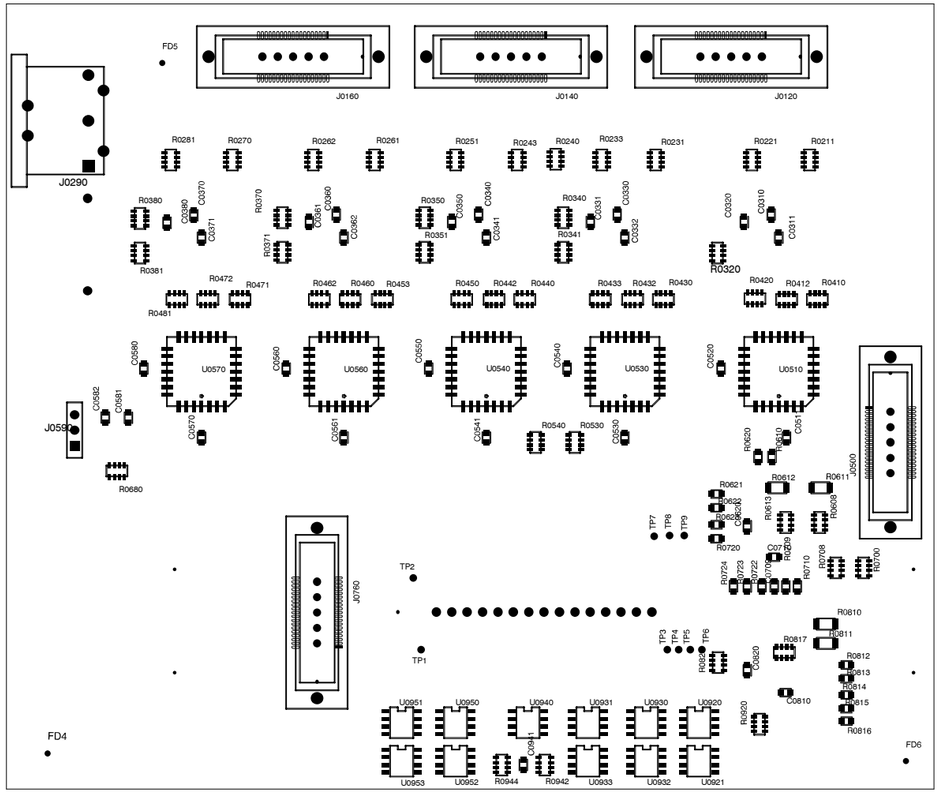
LOGIC1 A01 2


LA_AD<31..0>
J0240
VREFCG
VREFGC
LA_AD_STB0_INV
LA_AD_STB0
LA_AD_STB0#_INV
LA_C/BE0#
LA_C/BE1#
LA_C/BE2#
LA_C/BE3#
LA_AD_STB1
LA_AD_STB1#
LA_AD_STB1#_INV
LA_SERR#
LA_PAR
LA_PERR#
LA_PME#
LA_STOP#
LA_DEVSEL#
LA_TRDY#
LA_IRDY#
LA_FRAME#
VCC
VEE
GND1
GND2
GND3
GND4
GND5
NOTE: THESE PINS ARE NOT CONNECTED TO GROUND!!!
J0240
131-6753-00
131-7091-00
NOTE: THESE PINS ARE NOT CONNECTED TO GROUND!!!
+3.3V
LA_SBA<7..0>
LA_SB_STB_INV
LA_SB_STB
LA_SB_STB#_INV
LA_SBA<7>
LA_SBA<6>
LA_SBA<5>
LA_SBA<4>
LA_SBA<3>
LA_SBA<2>
LA_SBA<1>
LA_SBA<0>
VDD
VDDQ1.5
LA_RBF#
LA_WBF#
LA_ST2
LA_PIPE#
LA_ST0
LA_ST1
LA_REQ#
LA_GNT#
LA_CLK
LA_RST#
VCC3.3
LA_INTB#
LA_INTA#
LA_USB+
LA_USB-
5.0V
3.3VAUX
LA_OVRCNT#
12V

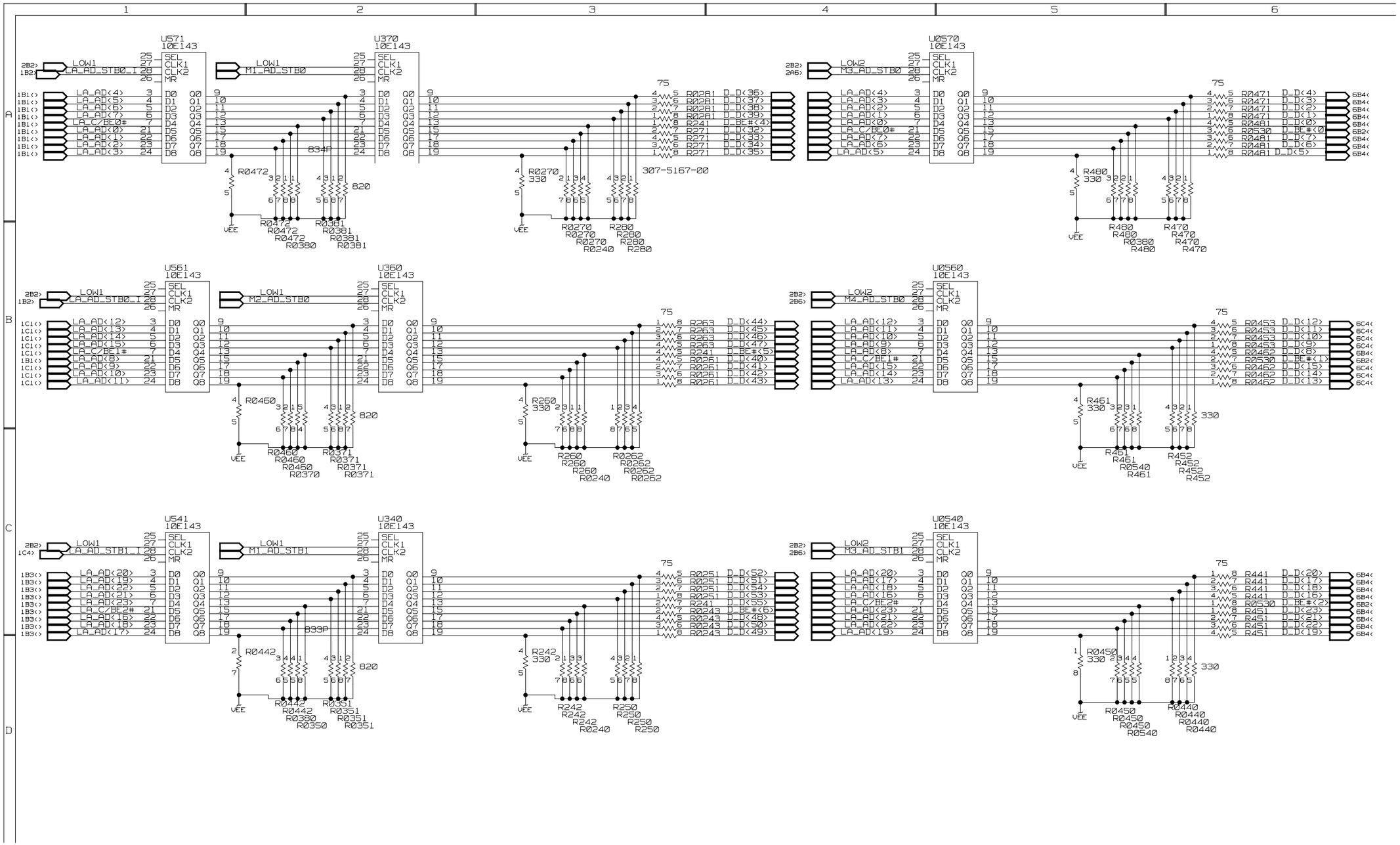
MICTOR 9



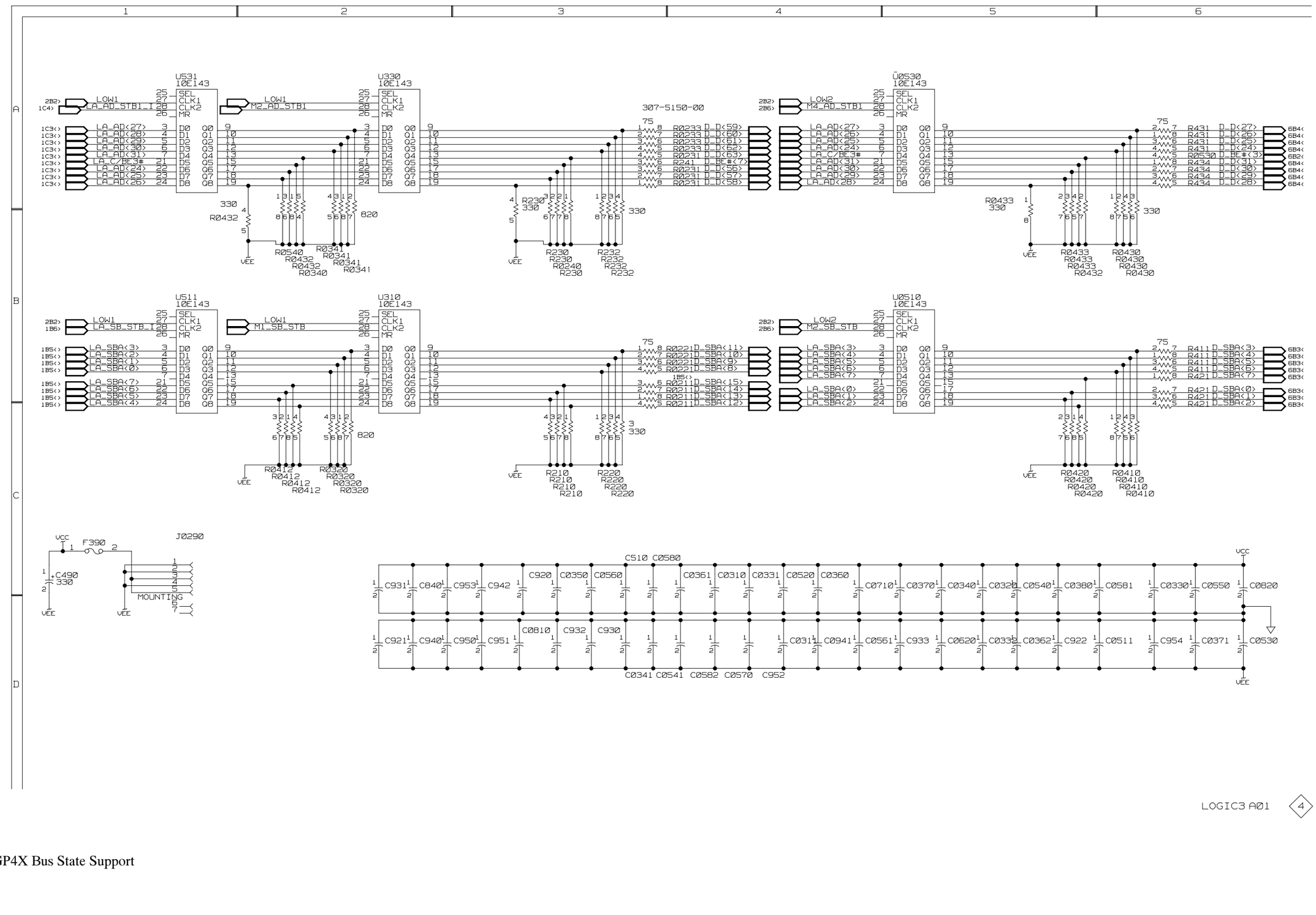
TMS 808 A1 Probe interface board (Front)



TMS 808 A1 Probe interface board (Back)


1
2
3
4
5
6
A
B
C
D
U571
10E143
U370
10E143
U0570
10E143
U561
10E143
U360
10E143
U0560
10E143
U541
10E143
U340
10E143
U0540
10E143
LOW1
LOW2
LA_AD_STB0_I
M1_AD_STB0
M3_AD_STB0
M2_AD_STB0
M4_AD_STB0
LA_AD_STB1_I
M1_AD_STB1
M3_AD_STB1
SEL
CLK1
CLK2
MR
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
LA_AD<4>
LA_AD<5>
LA_AD<6>
LA_AD<7>
LA_C/BE0#
LA_AD<0>
LA_AD<1>
LA_AD<2>
LA_AD<3>
LA_AD<12>
LA_AD<13>
LA_AD<14>
LA_AD<15>
LA_C/BE1#
LA_AD<8>
LA_AD<9>
LA_AD<10>
LA_AD<11>
LA_AD<20>
LA_AD<19>
LA_AD<22>
LA_AD<21>
LA_C/BE2#
LA_AD<16>
LA_AD<23>
LA_AD<18>
LA_AD<17>
75
834P
820
307-5167-00
833P
330
VEE
R0472
R0381
R0270
R280
R480
R470
R0460
R0371
R260
R0262
R0442
R0351
R242
R250
R450
R440
R461
R452
R0540
R441
R451
R0530

LOGIC2 A01 3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10E143
LOW1
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LA_AD<27>
LA_AD<28>
LA_AD<29>
LA_AD<30>
LA_AD<31>
LA_C/BE3#
LA_AD<24>
LA_AD<25>
LA_AD<26>
330
R0432
R0540
R0432
R0340
820
R0341
R0341
R0341
U330
10E143
LOW1
M2_AD_STB1
307-5150-00
R0233 D_D<59>
R0233 D_D<60>
R0233 D_D<61>
R0233 D_D<62>
R0231 D_D<63>
R241 D_BE#<7>
R0231 D_D<56>
R0231 D_D<57>
R0231 D_D<58>
R230
330
R230
R0240
R230
330
R232
R232
R232
U0530
10E143
LOW2
M4_AD_STB1
R0433
330
R0433
R0433
R0433
330
R0430
R0430
R0430
R0530
D_BE#<3>
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R0412
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R0320
R0320
R0320
U310
10E143
LOW1
M1_SB_STB
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R0221 D_SBA<10>
R0221 D_SBA<9>
R0221 D_SBA<8>
R0211 D_SBA<15>
R0211 D_SBA<14>
R0211 D_SBA<13>
R0211 D_SBA<12>
R210
R210
R210
R210
3
330
R220
R220
R220
R220
U0510
10E143
LOW2
M2_SB_STB
R0420
R0420
R0420
R0420
R0410
R0410
R0410
R0410
R411 D_SBA<3>
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R411 D_SBA<5>
R411 D_SBA<6>
R421 D_SBA<7>
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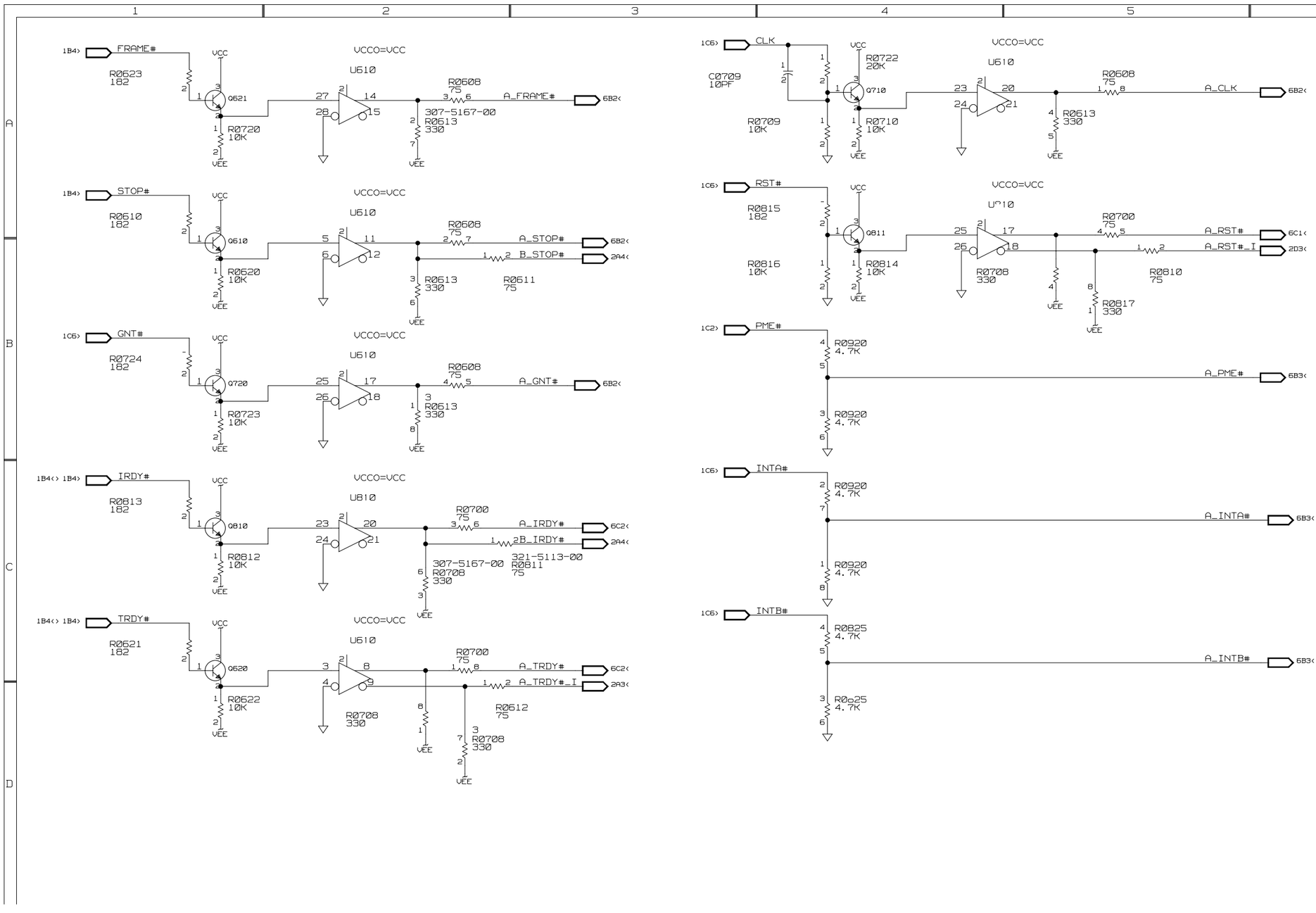
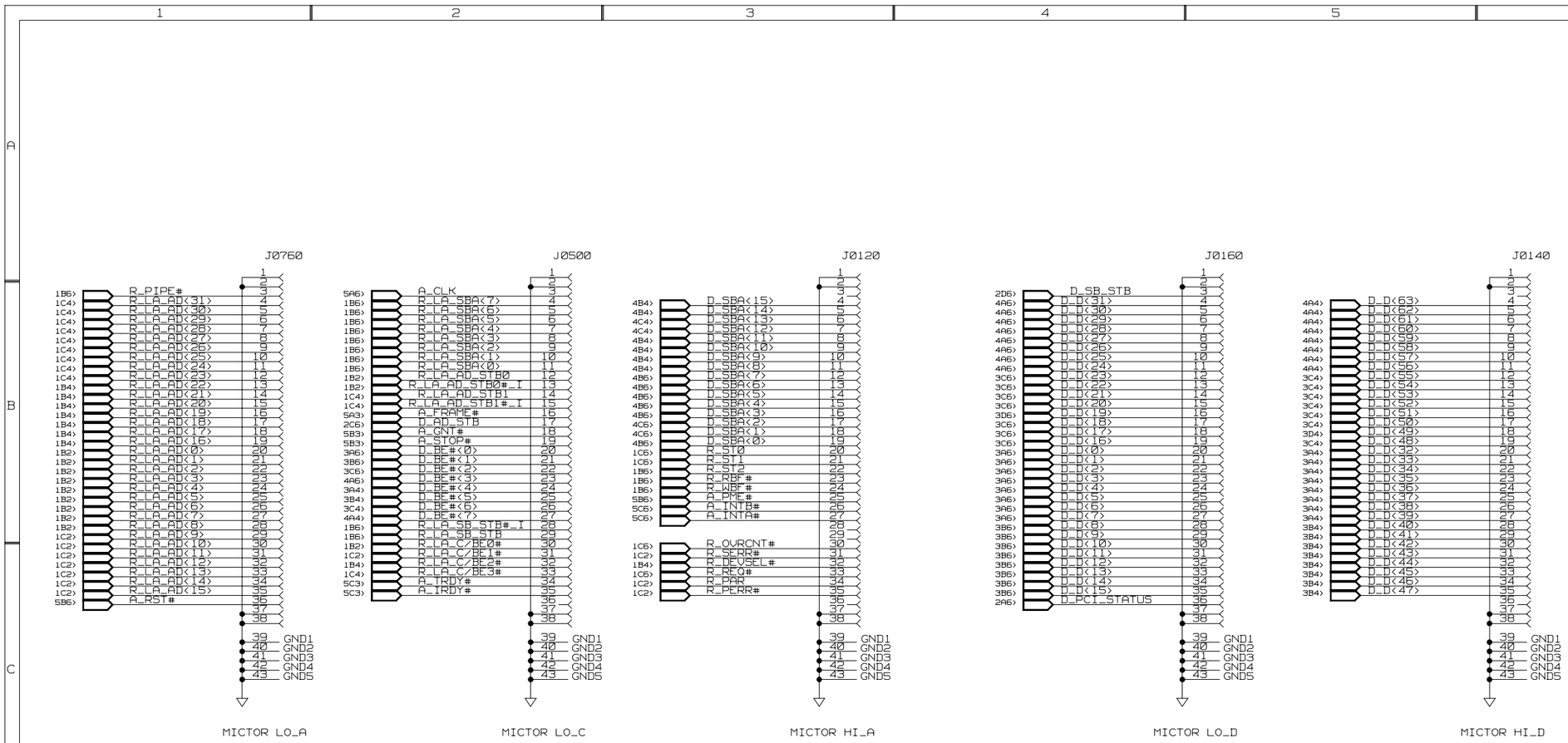
R421 D_SBA<2>
J0290
F390
C490
330
MOUNTING
C510 C0580
C931 C840 C953 C942 C920 C0350 C0560 C0361 C0310 C0331 C0520 C0360 C0710 C0370 C0340 C0320 C0540 C0380 C0581 C0330 C0550 C0820
C921 C940 C950 C951 C0810 C932 C930 C0311 C0941 C0561 C933 C0620 C0335 C0362 C922 C0511 C954 C0371 C0530
C0341 C0541 C0582 C0570 C952
LOGIC3 A01
4



LEVEL_SHIFT A01 5



MICTORS A01 6

Replaceable Parts List

Replaceable Parts

This section contains a list of the replaceable parts for the TMS 808 AGP4X bus support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105-3608
14310	AULT INC	7300 BOONE AVE NORTH BROOKLINE PARK	MINNEAPOLIS, MN 55428
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
61857	SAN-O INDUSTRIAL CORP	91-3 COLIN DRIVE	HOLBROOK, NY 11741
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001
82389	SWITCHCRAFT	DIV OF RAYTHEON 5555 N. ELSTON AVENUE	CHICAGO, IL 60630-1314
S3109	FELLER U.S. CORPORATION	72 VERONICA AVE UNIT #4	SOMERSET, NJ 08873
TK0303	FAB-TEK INC	324 CHRISTIAN ST	OXFORD, CT 06478
TK1373	PATELEC-CEM	10156 TORINO VAICENTALLO 62/456	ITALY,
TK2541	AMERICOR ELECTRONICS LTD	UNIT-H 2682 W COYLE AVE	ELK GROVE VILLAGE, IL 60007
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
5-0	010-0629-01			1	ADAPTER,PROBE:AGP4X,STATE,1.5V,TMS808 OPT 01	80009	010-0629-01
-1	671-5259-01			1	CIRCUIT BD ASSY:AGP4X EXTENDER,TMS808 OPT 01	80009	671-5259-00
-2	131-6269-00			1	CONN, EDGECARD:STRADDLEMNT, FEMALE, STR, 124 POS,0.039 CTR (1.0MM CTR),0.386 TAIL X 0.37 H,30 G	00779	145384-1
-3	131-7091-00			1	CONN,HDR:SMD,MALE,VERTICAL,114 POS,0 .025CTR,30 GOLD,MATCHED IMPEDANCE,MICTOR		1-767005-0
-4	671-4869-01			1	CIRCUIT BD ASSY:AGP4X, TMS808 OPT 01	80009	671-4869-00
-5	105-1089-00			5	LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,0.48 H X 1.24 L,W/PCB SINGLE CLIP,P6434	60381	105-1089-00
-6	131-6134-01			5	CONN,PLUG:SMD,MICTOR,PCB,FEMALE,STR,38 POS,0.025 CTR,0.245 H,GOLD,TLA7QS	00779	767054-1
-7	131-5449-00			1	CONN,CIRC DIN:PCB,FEMALE,RTANG,5 POS,ON 0.276 PIN CIRCLE,0.73 H X 0.140 TAIL,SHLD W/MTG HOLES	00779	520842-1
-8	131-4356-00			1	CONN,BOX:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER	26742	9618-302-50
-9	131-4530-00			1	CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,	00779	104344-1
-10	159-0059-00			1	FUSE,WIRE LEAD:5A,125V	61857	SPI-5A
-11	131-6468-00			1	CONN,RCPT:SMD,MICTOR,FEMALE,STR,114 POS,0.025 CTR,PDNI,0.236 H,MATCHED IMPEDANCE,50 OHM,S	TK0AT	767054-3
-12	129-1511-00			4	SPACER,POST:0.50 L,4-40,F/F,HEX,BRASS	55566	2057-440-B-5
-13	211-0028-00			8	SCREW,MACHINE:4-40 X 0.188,BDGH,NYL SLOT	85480	ORDER BY DESCRIPTION
					STANDARD ACCESSORIES		
	071-0560-03			1	MANUAL,TECH:INSTRUCTION,AGP4XT;TMS808	TK2548	071-0560-03
	----------			1	MANUAL, TECH: TLA 700 SERIES MICRO SUPPORT USER	80009	ORDER BY DESCRIPTION
	161-0104-00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,RTANG,IEC320, RCPT X STR,NEMA 15-5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION
	119-6377-00			1	POWER SUPPLY:40W,5VDC 8A OUT,100 VAC 47-63 HZ IN,DESKTOP,PFC,REGULATED,5.08L X 3.05W X 1.59H	14310	PW106MA0512Q01
					OPTIONAL ACCESSORIES		
	----------*			5	P6434 MASS TERMINATION PROBE, Opt 21 *	80009	ORDER BY DESCRIPTION
	161-0104-05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG, IEC320,RCPT,AUSTRALIA,SAFETY CONTROLLED	TK1373	161-0104-05
	161-0104-06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG, IEC320,RCPT,EUROPEAN,SAFETY CONTROLLED	TK1373	ORDER BY DESCRIPTION
	161-0104-07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10A,2.5 METER,RTANG, IEC320,RCPT X 13A,FUSED,UK,SAFETY CONTROLLED	TK2541	ORDER BY DESCRIPTION
	161-0167-00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10A,2.5 METER,RTANG, IEC320,RCPT,SWISS,NO CORD GRIP,SAFETY CONTROLLED	S3109	ORDER BY DESCRIPTION

*** See the P6434 manual for detailed replaceable part information.**

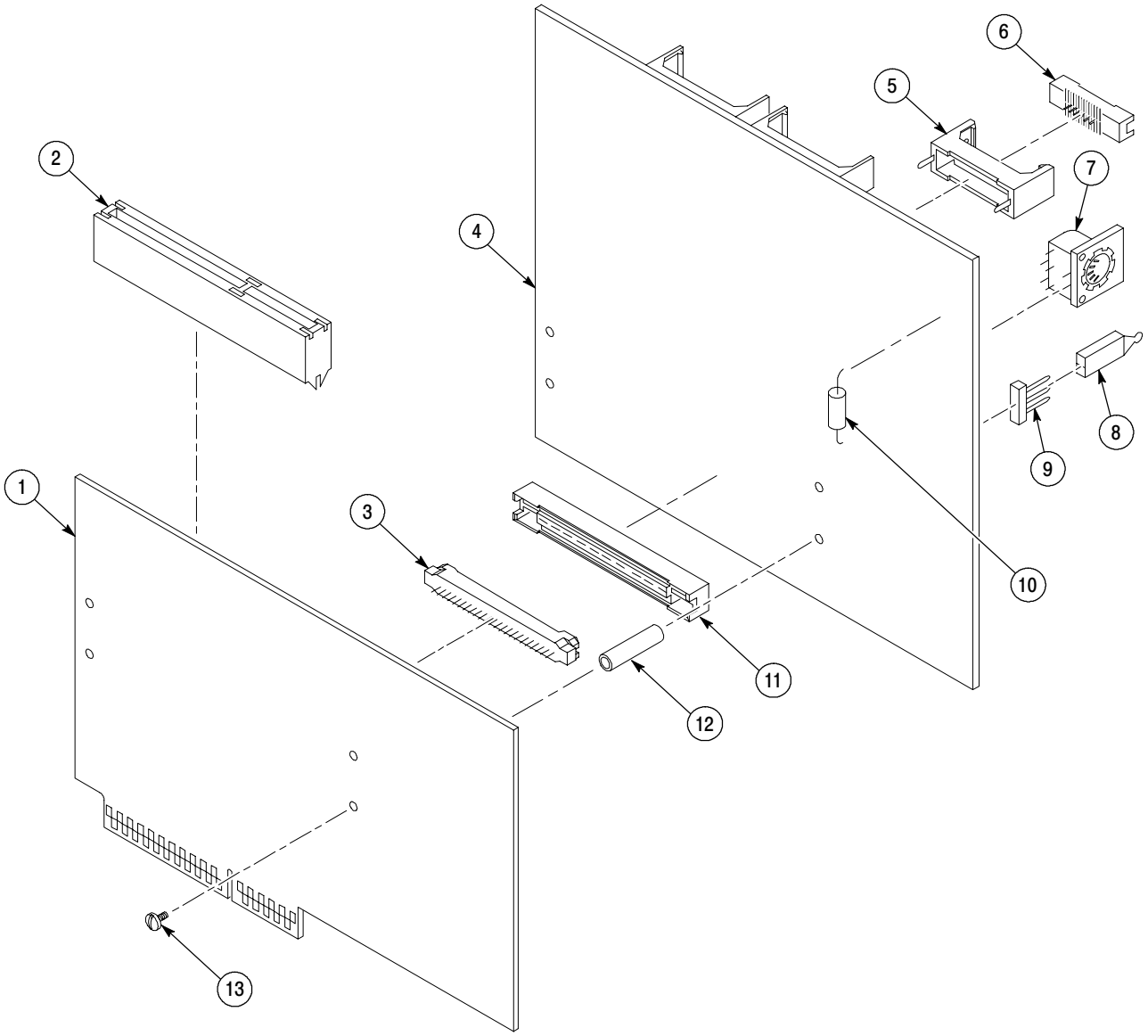


Figure 5- 1: AGP4X probe adapter exploded view

Index

Index

P

R

S

T

U

W